VOYAGER

SPACECRAFT Phase B, Task D

FINAL REPORT
OCTOBER 1967

Annex to
Volume 4, Spacecraft Electrical Subsystems Definition

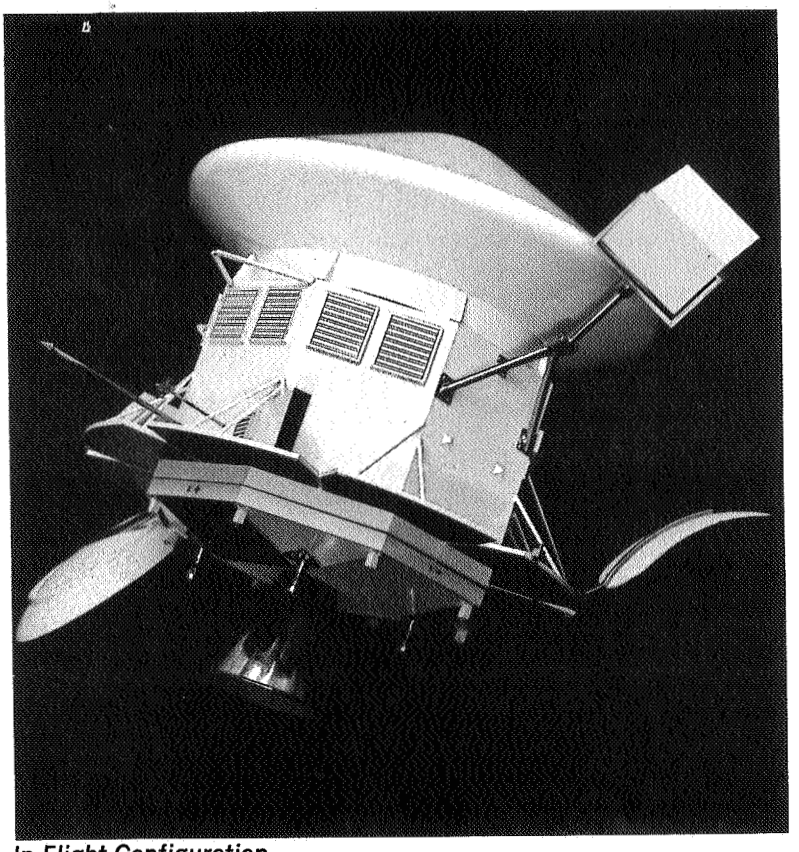
Prepared for
GEORGE C. MARSHALL SPACE FLIGHT CENTER
Huntsville, Alabama

Voyager Operations
Space Vehicles Division

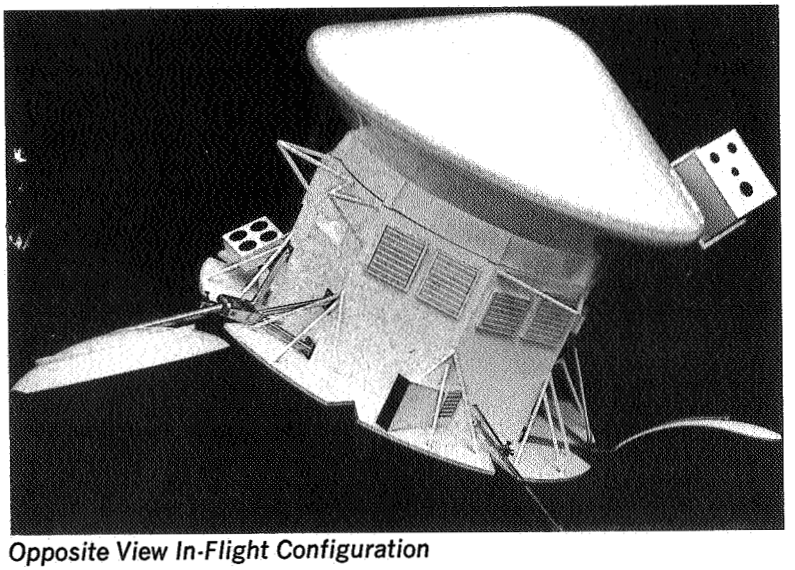
TRW SYSTEMS GROUP

One Space Park, Redondo Beach, California

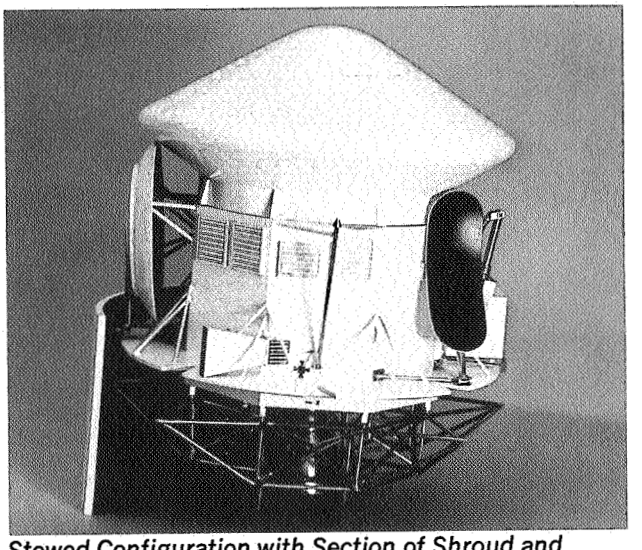
MODEL OF TRW RECOMMENDED VOYAGER SPACECRAFT



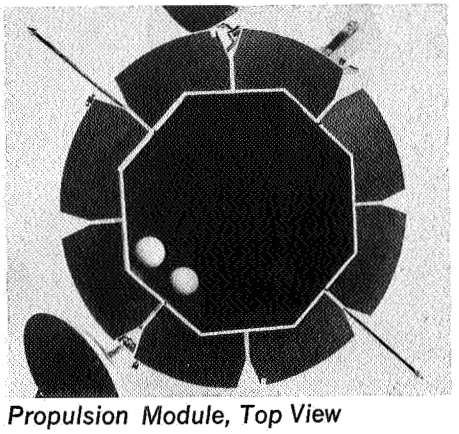
In-Flight Configuration



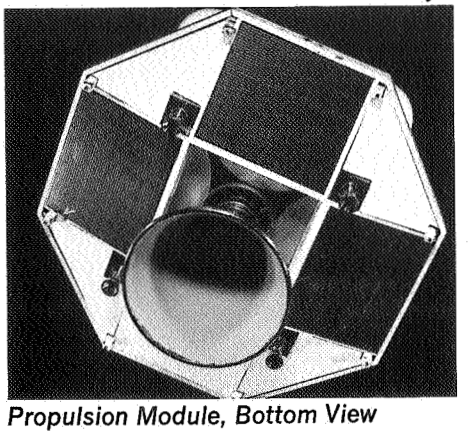
Opposite View In-Flight Configuration



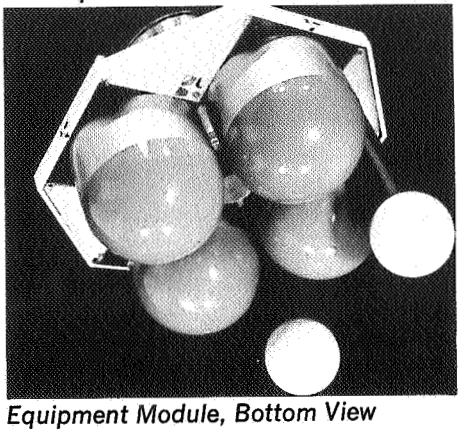
Stowed Configuration with Section of Shroud and Planetary Vehicle Adapter



Propulsion Module, Top View



Propulsion Module, Bottom View



Equipment Module, Bottom View

Copy 13

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APPENDIX A

MODULATION AND CODING

1. PCM VERSUS FM MODULATION

1.1 Introduction

The results of comparing two most widely used modulation techniques, pulse code modulation (PCM) and frequency modulation (FM) for transmission of Voyager video data is presented in this section. Comparisons were based on maximizing the picture-element transmission rate at the same picture quality, as represented by the output signal-to-noise ratio (SNR). The communication link is assumed to be power limited but not bandwidth limited.

1.2 Picture Quality and Output Signal-to-Noise Ratio

For a video signal, the criteria for establishing an acceptable level of output SNR is subjective. For television pictures, experiments have shown that high frequency noise is less objectionable to the viewer than low frequency noise (Ref. 1 and 2). Hence, for a given SNR, the picture quality is dependent on the spectral distribution of the video noise. To eliminate this ambiguity, the concept of "weighted noise" was used. The weighted noise is defined as video noise measured with a weighting network which represent the spectral perception of noise by an average viewer. The weighting characteristic is a function of the type of television system. For example, the weighting characteristics of the American 525-line system is such that the video noise power is reduced by 6 db for AM, 10 db for FM without pre-emphasis, and 12.4 db for FM with pre-emphasis. Whereas, for 625-line European system, the noise power is reduced by 8.5 db for AM and 16 db for FM.

The weighting factor for the Voyager video system is yet to be determined. As a take-off point, it is possible to analyze a tradeoff between picture quality as represented by the unweighted output SNR and picture element transmission rate.

Before performing the analysis, the output SNR must be defined. In most studies of TV picture quality, it is generally taken as the ratio of

peak-to-peak signal power to RMS noise power. To conform with the normal usage and provide an easy means of comparison, this same definition will be used.

1.3 Frequency Modulation System

For a FM system operated above threshold, the output SNR is related to the maximum video signal frequency f_m as follows:

$$SNR = 3(2\beta)^2 \frac{B}{f_m} C/N_i \qquad (A-1)$$

where

- SNR = ratio of peak-to-peak signal power to RMS noise
- β = modulation index, which is equal to the ratio of peak frequency deviation to the highest video signal frequency
- B = predetection bandwidth
- f_m = postdetection bandwidth and is taken to be equal to the highest video signal frequency
- C = total input signal power
- N_i = RMS noise power in predetection bandwidth B

In addition to Equation (A-1), two more relationships are needed to determine the highest video frequency. Due to the threshold phenomena of the FM system, Equation (A-1) will be valid only for a minimum C/N_i which is termed FM threshold, T_H, and is related to the predetection bandwidth and receiver noise temperature. For a given receiving system, T_H uniquely determines the upper bound of the predetection bandwidth as follows:

$$B = \frac{C/\phi}{T_H} \qquad (A-2)$$

where ϕ is the predetection noise power spectral density.

The second relationship is Carson's rule which defines the minimum predetection bandwidth required to keep the FM distortion to a satisfactory level:

$$B = 2f_m(1 + \beta) \qquad (A-3)$$

Noting that picture element transmission rate is twice f_m, then Equations (A-1), (A-2), and (A-3) can be used to determine the picture element transmission rate for a given C/ϕ, T_H and SNR. The solution of these equations can be obtained by noting that C/N_i and B should satisfy all three equations at threshold. The solution for f_m can be obtained by first determining β by solving the three simultaneous Equations (A-1), (A-2), and (A-3). By this procedure, a cubic equation of β is obtained:

$$\beta^2 (1 + \beta) = \frac{SNR}{T_H} \frac{1}{24} \qquad (A-4)$$

Solution for β can be obtained either by graphical method or by iteration. Then from Equations (A-2) and (A-3) predetection bandwidth B and picture elements transmission rate, $2f_m$ can be obtained respectively. Using a normalized value of 57 db for C/ϕ, the picture transmission rate as a function of various SNR and T_H are shown in Figure A-1.

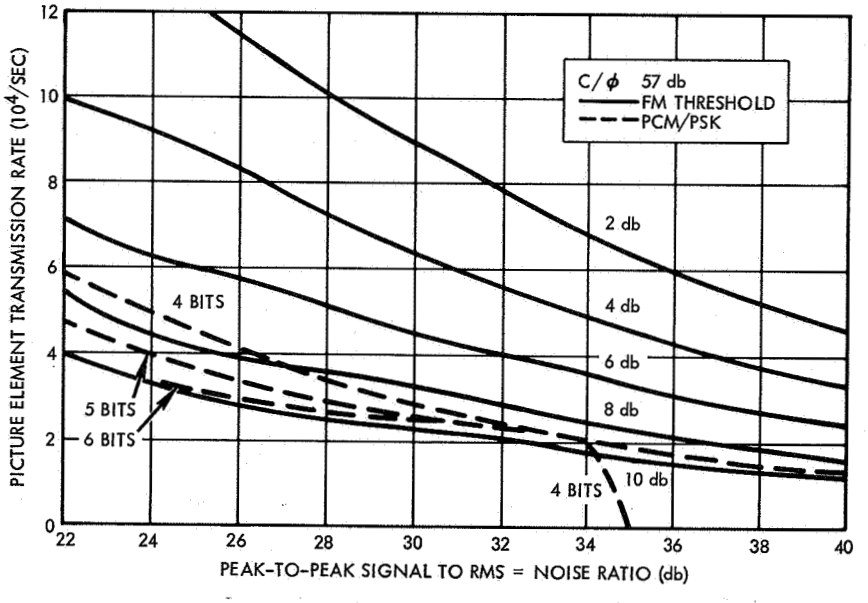

Figure A-1. Maximum Picture Element Transmission Rate

1.4 PCM/Phase Shift Keying

For a PCM system, the output SNR is related to the quantitization level m (in bits) and bit error rate P_e as follows:[3]

$$SNR = \frac{3}{P_e (1 - 4^{-m}) + 4^{-(m+1)}} \qquad (A-5)$$

For a given SNR and m, the bit error rate P_e can be calculated and then from P_e, the maximum bit rate bandwidth can be obtained. For example, for m equal to 5, the maximum bit error rate can be determined as follows:

$$P_e \frac{1 - SNR\ 4^{-(m+1)}}{SNR\ (1 - 4^{-m})} = \frac{1 - 1.6 \times 10^3 \times 2.4 \times 10^{-4}}{1.6 \times 10^{-3}} = 3.86 \times 10^{-4} \qquad (A-6)$$

Then for bit error rate of 3.86×10^{-4}, and using coherent PSK, the SNR in bit rate bandwidth B_o should be 7.5 db or

$$\frac{C/\phi}{B_o} = 5.6 \qquad (A-7)$$

$$B_o = \frac{C/\phi}{5.6} \qquad (A-8)$$

The maximum picture element transmission rate is equal to bit rate divided by quantitization level. The results of such a calculation of the maximum picture element transmission rate as a function of SNR and quantitization level of m = 4, 5, and 6 are also plotted in Figure A-1.

1.5 Voyager Design Considerations

As indicated in Figure A-1, FM with threshold extension is better than PCM/PSK system. However, in case of PCM, it is also possible to use coding to trade bandwidth for power, as in the case of FM. As shown in Section 2, of this Appendix, the amount of improvement in data transmission capability by coding is dependent on the error rate probability and the coding scheme. The coding scheme recommended for Voyager application, (32, 6) biorthogonal coding, improves the transmission rate by 4 db at an error rate probability of 10^{-3}. At this error rate, SNR's are

approximately 32, 34 and 35 db for quantitization level m = 4, 5, and 6. At these output SNR's, the transmission capability of the coded PCM is approximately equivalent to FM with threshold at 4 db.

In addition to theoretical consideration, current hardware capability must also be weighted in chosing a modulation method for the Voyager application. At the present, an FM demodulator with threshold of 4 db is possible, but achievement is difficult. A more reasonable threshold is 6 db. For the PCM case, equipment imperfection will also prevent a system from realizing its full potential; the degradation is probably in the order of 2 db. Thus, FM with threshold extension and PCM with (32, 6) encoding essentially have the same picture element transmission capabilities. The PCM case is clearly superior, however, when data rate reduction by tape recorder is required as is the present case. After playback at a reduced speed, the tape recorder can preserve the recorded data with high fidelity in the digital form much more easily than in analog form. This phenomena is much more pronounced at high reduction ratios; such a reduction will be required in a failure mode where link capability is reduced considerably. For these reasons, PCM with coding is recommended for the application to Voyager baseline system.

2. CODING CONSIDERATIONS

2.1 Introduction

The coding systems presented here are designed to achieve a certain reliability in the transmission of telemetry data at a low cost in power. The cost that is involved is either in bandwidth or in information rate. There are several coding systems currently in various stages of design and implementation on projected space missions which achieve this purpose with varying degrees of complexity and expense. The decoders which are ground based are not limited by size, and have basically only the realtime requirements for coding. The encoders which are on board the spacecraft must of course be simple and compact. Two such systems are discussed and alternate proposals are presented.

2.2 Self-Synchronizing Biorthogonal Code

This coding system is currently being implemented on Mariner '69. It is, as far as coding systems go, a classical system, since prototypes have been engineered and its capabilities thoroughly analyzed. In particular, all that is necessary to know of the coding system may be found in various portions of Reference 4. References to this text cite the necessary figures and computations.

2.2.1 Encoding

Six data bits are encoded into a 32-bit code word of the biorthogonal code. A six stage shift register is used with the recursion rule.

$$A_{n+6} = A_{n+5} + A_{n+3} + A_{n+2} + A_{n+1} + A_n \qquad \text{(A-9)}$$

$$n = 0, 1, 2, \ldots 25$$

The 32nd bit A_{31} is given by the rule

$$A_{31} = A_0 + A_2 + A_5 \qquad \text{(A-10)}$$

or alternately,

$$A_{31} = \sum_{i=0}^{30} A_i \qquad \text{(A-11)}$$

Before transmission, a fixed 32-bit word C_5

$$C_5 = (101010101 \ldots 011) \qquad \text{(A-12)}$$

is added mod 2 to the word for self-synchronizing capability. The encoding techniques here is not the one listed in Reference 4, page 147, but is an alternate mechanizable procedure, with analogous properties. Recently, Dr. Rumsey of JPL has announced the discovery of a comma-free vector C_5 which gives a better sync capability.

2.2.2 Decoding

The technique used here is maximum likelihood decoding. The received word is correlated with all possible code words, using an analog cross-correlator and the decoder chooses the word with maximum correlation (Section 7.2, Ref. 4). This is the optimal decoding procedure, and minimizes the probability of error.

2.2.3 Properties of the Code

The (32, 6) biorthogonal code has a minimum distance of 16 bits, giving it an error correction capability of at least 7 bits. The technique of decoding here, using the whole word (avoiding quantization errors on the bits), is an optimal one. The self-synchronizing ability for word-frames comes from adding the vector C_5 (see above) to the code, achieving a degree of comma-freedom equal to 6 bits; i.e., if we were to start decoding from the wrong position, the word would appear to have at least 6 errors. In fact, by decoding 36 words at all 32 possible positions, one can achieve the correct synchronous position with a probability of 0.999 at the required signal power.

From the Tables of Viterbi, coded transmission effects a saving of 2.5 db in signal power to achieve the same probability of error as uncoded transmission. The proposed JPL system is designed to transmit at 2.5 db per information bit, and achieve a probability of bit error $\sim 5 \times 10^{-3}$.

2.3 Convolutional Coding

A second system currently being implemented aboard the Pioneer missions is a rate 1/2 convolutional code, using sequential decoding techniques. As envisaged in the description of Lumb and Hoffman (Ref. 5), the basic (50, 25) code gives a 4.1-db gain over the parity check code scheme currently used. This system is more complicated than the biorthogonal code and requires the SDS computer on the ground for the decoding process. However, a special purpose computer (complete cost estimate by Codex Corporation at 10 k) can be used. As described in the referenced memo, the convolutional code actually works on fixed block length both to achieve synchronization and to facilitate

decoding. Each block is 224 bits long, and has 14 final bits of the Barker code type for frame synchronization and decoding. Thus, the actual rate is slightly less than 1/2.

2.3.1 Encoding

Twenty-five information bits are put into a shift register of the same length, and a parity check is generated. Shift the information positions to the right, drop the right-most one, enter the next information bit, and generate another parity check. The initial stage of the register is of course known (perhaps all 0).

The bits to be transmitted are information, parity, information, parity, etc., with each parity check acting on the preceding 25 bits. Thus, the encoding device is a simple one, with the sync modification mentioned above.

2.3.2 Decoding

Before going into the details of the decoding algorithm, note that the telemetry data is to be furnished in blocks of 6 bits, plus a seven parity check on these. Thus, there is an additional error correcting aid.

Each received bit as detected by the matched filter detector of the phased key signal is quantized to 3 bits, thus effectively furnishing an 8-letter alphabet to be used in the code. The decoding algorithm used is the one described in Reference 6. Since sequential decoding is relatively unfamiliar to many, the basic techniques are outlined here.

Assume that there is a correct message and the next information bit and parity check come in. As quantized, there is a 6-bit pair (3 information, 3 check bits). For the eight possible check symbols, a set of transition probability is assigned and stored in the table lookup. These are the probabilities that a symbol was received, given that a 0 or 1 was transmitted.

This data is stored in memory for use by the decoding in a table lookup form. As each information/parity pair is selected for decoding, a table lookup operation is performed to determine two metric values for that pair, one assuming a 0 was input into the spacecraft encoder and the other assuming that a 1 was input into the encoder. The decoder computes

the correct information/parity combination by using an encoder configuration identical to that of the spacecraft and the previous 24 decoder bit-decisions.

The metric used for the computation is: (Ref. 5)

$$\log_2 \left[\frac{\text{transition prob (info)}}{\text{prob of receiving (info)}} \times \frac{\text{transition prob (parity)}}{\text{prob of receiving (parity)}} \right] - \text{bias}$$

The most likely choice (the one with the highest metric value) is selected and the corresponding bit is inserted into the decoder's shift register. Its metric value is then added to the total of the metrics of the previous decisions for the frame being decoded.

Because of noise on the channel, it is possible that one (or more) of the information/parity pairs will appear as an incorrect bit. An incorrect decision will be made by the decoder, and a bit which is in error will be inserted into the shift register. However, since the bits in the decoder shift register do not match those that were in the encoder, the succeeding sequence of parity bits generated by the decoder will not correspond to those sent by the encoder. This discrepancy shows up quickly since few of the channel symbols received will closely match those generated by the decoder as possible choices. These bit choices will have small or negative metric values, and the total metric will fall below a predetermined threshold. When this happens, the decoder recognizes a possible error condition and enters a search mode. (It is also possible that the decoder is proceeding correctly, but that noise has caused the metric value to drop below the threshold.)

In the search mode, the decoder executes a systematic search through the tree of possible information/parity sequences in order to find a better fit to the received sequence, if one exists, before the decoding process is allowed to continue. The threshold value is lowered in fixed increments, and the tree is searched according to a set of rules in order to find a valid path whose total metric never falls below that threshold. In doing so, it may make decisions to select the second best choice for information/parity pairs that might have been received in error. As soon as the decoder decides on a new path (or arrives back at the old path with

a lower threshold), the search mode is left and the decoding process continues as before. As the decoding proceeds successfully, the threshold value is raised in fixed increments (always remaining below the total value of the metric) so that possible error conditions may be detected most quickly.

The structure of the Pioneer format is such that much is known about the data as it is received from the spacecraft. Information bits are arranged into groups of seven to form data words. With certain exceptions, the 7th bit of each word is a parity check on bits 1, 3, and 5. Data words are organized into frames of 32 words where words 1 and 17 are always a fixed frame sync word (Barker word) and its complement and word 2 is a mode identification.

Use of this information is made by the sequential decoder subroutine module of the station program to:

1) Provide frame synchronization for the entire program

2) Locate the starting point to begin the decoding process

3) Force the decoding process where the path is known in order to speed the computation and reduce the probability of undetected errors.

Because sequential decoding has an inherently variable decoding rate, several restrictions have been imposed to determine the point at which decoding should be suspended and further attempts made at some subsequent time, off-line.

Since code resynchronization occurs at one frame intervals, decoding is done by the computer one frame at a time. Data is continually input and buffered by the computer for processing via an interrupt system as each information/parity pair appears in the computer buffer. If one complete frame is input before the previous frame is decoded, that frame is abandoned and the decoder proceeds immediately to the most recent frame.

2.4 Concatenated Codes

An alternate coding procedure to the ones previously mentioned is the concatenated coding scheme of Forney (Ref. 6), which is a more

powerful error correcting procedure than the ones mentioned, and gives additional burst error protection. The coding consists of concatenating a biorthogonal code with a Reed-Solomon code and two different decoding techniques are applied. This class of codes is very efficient, and is a means of achieving the Shannon Bound.

One possible self-synchronizing concatenated code is a (31, 14) R-S code concatenated with a (16, 5) biorthogonal code which achieves a final probability of error $<5 \cdot 10^{-3}$ for a signal-to-noise ratio of 2 db.

2.4.1 Encoding

The code is a code of rate $14/31 \cdot 5/16$ of length $31 \cdot 16$ binary symbols with 70 information bits. It is composed of an inner code and an outer code. The basic encoding diagram is as follows.

INFORMATION BITS → OUTER CODE → INNER CODE →

2.4.1.1 Outer Code

The 70 bits of information are considered as 14 blocks of 5-bit symbols, each symbol representing an element in $GF(2^5)$*

$$\overset{\alpha_0}{a_0, a_1, a_2, a_3} \qquad \overset{\alpha_1}{a_4, a_5, a_6 \cdots a_9} \qquad \overset{\alpha_2}{a_{10} \cdots a_{14}} \tag{A-13}$$

Encode

$$\alpha_0, \alpha_1 \cdots \alpha_{13} \rightarrow \alpha_0, \alpha_1, \alpha_2 \cdots \alpha_{13}, \alpha_{14} \cdots \alpha_{30} \tag{A-14}$$

via the recursion rule

$$f(x) = \prod_{i=0}^{14} (x + \lambda^i) = x^{14} + \mu_{13} x^{13} + \mu_{12} x^{12} + \cdots + \mu_0 ; \tag{A-15}$$

$$\lambda^5 + \lambda^2 + 1 = 0$$

*GF( ) refers to a Galois field.

or

$$\alpha_{n+14} = \sum_{i=0}^{13} \mu_i \alpha_{n+i} \qquad \text{(A-16)}$$

Add the vector $\{x^{15};\ x = \lambda^0, \lambda^1, \lambda^2 \cdots\}$ to a full word as a sync comma-free vector (Ref. 7)

2.4.1.2 Inner Code

Each (α_i) of the (31, 14) code is now considered as a 5-bit word, and is encoded into a 16-bit code word A_i of the (16, 5) biorthogonal code as in Section 2.2.

$$\alpha_0, \alpha_1 \cdots \alpha_{30} \rightarrow A_0, A_1 \cdots A_{30} \qquad \text{(A-17)}$$

In essence, a $(16 \cdot 31)$ binary word is sent. Note, the (16, 5) comma-free code is found by adding the vector C_4 (Ref. 4, p. 47) to the (16, 5) biorthogonal code.

2.4.2 Decoding

The decoding techniques for both these codes are very simple. First decode the inner code, and then the outer one.

2.4.2.1 Inner Code

This is a (16, 5) biorthogonal code. Each A_i is fed into a correlation detector where it is compared to all 32 possible code words. Using the comma-freedom and maximum likelihood decoding, a decoding symbol is obtained for use in the outer code. There is also symbol synchronization as in Section 2.2. A set of symbols emerges after decoding, $\alpha_0, \alpha_1, \alpha_2 \cdots \alpha_{30}$ which is a word of the (31, 14) code over $GF(2^5)$.

2.4.2.2 Outer Code

There is a self-synchronizing (31, 14) R-S code which may correct up to 9 errors. However, we shall correct up to 50 symbol errors in $GF(2^5)$. The table for $GF(2^5)$ is generated by the rule, $\lambda^5 = \lambda^2 + 1$. The decoding algorithm now follows.

1) Compute

$$\sum_{i=0}^{30} \alpha_i \lambda^i = S_1 \tag{A-18}$$

$$\sum_{i=0}^{30} \alpha_i \lambda^{2i} = S_2 \tag{A-19}$$

$$\sum_{i=0}^{30} \alpha_i \lambda^{10i} = S_{10} \tag{A-20}$$

2) If $S_i = 0$ $i = 1, 2, 3 \ldots 10$, the received word is pronounced correct.

3) If some $S_i \neq 0$, then we compute

$$T_1 = S_3 S_1 S_2^2 \tag{A-21}$$

If $T_1 \neq 0$, one error has been made in the ℓ^{th} position, where $S_2/S_1 = \lambda^{\ell}$. The error committed is S_1^2/S_2. Add the value S_1^2/S_2 to the ℓ^{th} position.

4) If $T_1 \neq 0$, we evaluate T_2

$$T_2 = \det \begin{vmatrix} S_3 & S_2 & S_1 \\ S_4 & S_3 & S_2 \\ S_5 & S_4 & S_3 \end{vmatrix} \tag{A-22}$$

If $T_2 = 0$, then 2 errors have been made, and the error positions k are given by λ^{ℓ}, λ^{k} roots of $x^2 + x\sigma_1 + \sigma_2 = 0$

$$\sigma_1 = \frac{S_3 S_2 + S_1 S_4}{T_1} \qquad \sigma_2 = \frac{S_3^2 + S_1 S_4}{T_1} \tag{A-23}$$

The errors $\hat{\alpha}_1, \hat{\alpha}_2$ made in the positions λ_1, λ_2 are given by

$$\hat{\alpha}_1 = \frac{S_1\lambda_2^2 + S_2\lambda_2}{\sigma_1\sigma_2} \qquad \text{(A-24)}$$

$$\hat{\alpha}_2 = \frac{S_2\lambda_1 + S_1\lambda_1^2}{\sigma_1\sigma_2}$$

5) If $T_2 \neq 0$, we assume three errors have been made in positions ℓ, k, m, where $\lambda_1 = \lambda^{\ell}$, $\lambda_2 = \lambda^{k}$, $\lambda_3 = \lambda^{m}$, are roots of the cubic equation

$$x^3 + x^2\sigma_1 + x\sigma_2 + \sigma_3 = 0 \qquad \text{(A-25)}$$

where the σ_i are solutions of the three linear equations

$$\begin{aligned} S_4 &= S_3\sigma_1 + S_2\sigma_2 + S_1\sigma_3 \\ S_5 &= S_4\sigma_1 + S_3\sigma_2 + S_2\sigma_3 \\ S_6 &= S_5\sigma_{\ell} + S_4\sigma_2 + S_3\sigma_3 \end{aligned} \qquad \text{(A-26)}$$

and the errors $\hat{\alpha}_i$ are solutions to

$$\begin{aligned} \Sigma\hat{\alpha}_i\lambda_i &= S_1 \\ \Sigma\hat{\alpha}_i\lambda_i^2 &= S_2 \\ \Sigma\hat{\alpha}_i\lambda_i^3 &= S_3 \end{aligned} \qquad \text{(A-27)}$$

6) For 4 and 5 errors, the algebra becomes slightly more complicated, but the method is analogous; i.e., we must solve the quartic

$$x^4 + \sigma_1 x^3 + \sigma_2 x^2 + \sigma_3 x + \sigma_4 = 0 \quad \text{when } \sigma_i \text{ are}$$

solutions of the four linear equations

$$\begin{aligned} S_5 &= S_4\sigma_1 + S_3\sigma_2 + S_2\sigma_3 + S_1\sigma_4 \\ S_6 &= S_5\sigma_1 + S_4\sigma_2 + S_3\sigma_3 + S_2\sigma_4 \\ S_7 &= S_6\sigma_1 + S_5\sigma_2 + S_4\sigma_3 + S_3\sigma_4 \\ S_8 &= S_7\sigma_1 + S_6\sigma_2 + S_5\sigma_3 + S_4\sigma_4 \end{aligned} \qquad \text{(A-28)}$$

Explicit formulas are easily obtained by actual computation. Mechanization and computations of the algebra may be found in Bartee and Schneider (Ref. 8). Synchronization is obtained by adding the comma-free vector and by decoding a finite number of words in each portion (Ref. 7).

2.5 ALTERNATE CONCATENATED CODE

Note that by concatenating a (21, 9) R-S code over GF(2^6) with the (32, 6) biorthogonal code in Section 2.2, one obtains a self-synchronizing code at 7/3 the bandwidth expansion, and lowers the signal-to-noise ratio requirements to less than 2-db per information bit.

The outer code is the R-S comma-free code generated by

$$f(x) = \prod_{i=0}^{8} (x + \lambda^i), \qquad \lambda = \beta^3 \qquad \beta^6 = \beta + 1 \qquad \text{(A-29)}$$

with comma-free vector

$$\{x^9; \quad x = \lambda^i \quad i = 0, 1 \cdots 20\} \qquad \text{(A-30)}$$

Up to five errors are corrected, in a manner similar to the previous concatenated code. The inner code is the biorthogonal comma-free code mentioned in Section 2.2.

3. REFERENCES

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APPENDIX B

METRIC ANALYSIS

1. INTRODUCTION

In the case of ranging, the receiving and transmitting bandwidths are defined by the spectrum occupancy of the pseudo-random noise ranging sequence. The primary tradeoff involved in handling the ranging signal is in selecting the best method of turning around the ranging code. The tradeoff between the two methods (code reconstruction and direct turnaround) is discussed in Section 2 below.

Range rate requires coherent carrier reception and retransmission. It also defines the receiver phase lock parameters required to track the Doppler frequency shift and rate of change of frequency shift. Section 3 analyzes the spacecraft and ground receiver phase lock parameters required to track the Doppler perturbed carrier frequency.

2. RANGING DIRECT TURNAROUND VERSUS CODE RECONSTRUCTION

The following assumptions have been made. In all cases the 210 foot ground antenna with 100 kilowatts of transmitter power is assumed. Also, the TRW recommended vehicle is assumed. The only service on the uplink is ranging, while on the downlink engineering telemetry (512 bits/sec) is transmitted simultaneously with ranging. The required subcarrier power-to-noise density is shown below in Table B-1.

Table B-1. Required Subcarrier Power-to-Noise Density Ratios

		Subcarrier Power-to-Noise Density db x Hz
Uplink		
Ranging	22 db in 2 B_{LO} = 0.8 Hz	21.0
Carrier	8 db in 2 B_{LO} = 20 Hz	21.0
Downlink		
Engineering telemetry 512 bits/sec		30.1
Ranging	22 db in 2 B_{LO} = 0.8 Hz	21.0
Carrier	6 db in 2 B_{LO} = 12 Hz	16.8
	6 db in 2 B_{LO} = 48 Hz	22.8

The smaller ground loop bandwidth is assumed when the vehicle omni antenna is used, while the larger loop is assumed when either the vehicle medium-gain or high-gain antenna is used.

The most up-to-date numbers for received signal power-to-noise density ratio were used. The received signal power-to-noise density ratio, S/Φ, can be written as

$$\frac{S}{\Phi} = C - 20 \log_{10} R$$

The constant C for both the uplink and the downlink for all three antennas is shown in Table B-2.

Table B-2. Received Power-to-Noise Density Constants - C

	Omni	Medium	High
Uplink	82.1	115.9	121.9
Downlink	62.6	95.6	101.6

The ranging modulation index on the uplink is set at 0.78 radian. The downlink modulation indices were optimized and are listed in Table B-3.

Table B-3. Optimum Modulation Indices

	Omni		Medium and High Gain	
	B_{PRN}	B_{Tel}	B_{PRN}	B_{Tel}
Turn-around	0.78	1.3	0.58	1.3
Regeneration	0.47	1.45	0.47	1.45

For the vehicle regeneration case the calculations are straightforward. In all cases the downlink limits the performance. For the turnaround ranging case, the effects of turnaround noise must be evaluated.

One of the important factors influencing the effect of ranging performance, with turn-around ranging, is the degradation due to turn-around noise.

Remodulation of the uplink spectrum onto the downlink carrier by the turnaround ranging channel in the spacecraft transponder effects the performance of the downlink communications in two important ways. First, the available transmitter power for downlink communication services is reduced by modulation of the downlink carrier by the uplink spectrum. Only the pseudo-random noise code is desired downlink information, while the uplink subcarriers and thermal noise are not and waste downlink power. Second, the uplink thermal noise appears in the downlink carrier sidebands and is detected at the ground receiver so that the effective ground receiver noise spectral density is increased. The magnitudes of these two effects are given by

$$\text{Downlink transmitter power reduction} = e^{-\sigma_n^2}\left[\sum_{i=1}^{N} J_o^2(\phi_i P)\right] \quad \text{(B-1)}$$

$$\text{Effective noise spectral density of ground receiver} = \Phi_g + \frac{\left[1-e^{-\sigma_n^2}\right]S_g}{B_v} M_c\left[\sum_{i=1}^{N} J_o^2(\phi_i)\right]\cos^2\theta'_{DL} \quad \text{(B-2)}$$

where

σ_n = rms noise modulating downlink carrier

ϕ_i = effective downlink modulation index of uplink subcarriers

θ'_{DL} = effective downlink modulation index of pseudo-random noise code

M_c = carrier modulation loss due to downlink communication services

S_g = received signal strength at ground receiver

Φ_g = ground station noise spectral density in absence of turnaround noise

B_v = effective bandwidth of uplink noise modulating downlink carrier (equal to turnaround ranging channel noise bandwidth).

Values, in terms of uplink parameters for the rms noise and effective subcarrier indices, σ_n and ϕ_i, are given in the following equations. The equations assumed that the downlink pseudo-random noise modulation index is set under strong signal conditions.

$$\phi_i = \left[2 \frac{J_1(\beta_i)}{J_o(\beta_i)} \right] \frac{\alpha_s \theta_{DL}}{\tan \theta_{UL}} \tag{B-3}$$

$$\sigma_n = \left[\frac{\sqrt{\frac{B_V}{B_L}}}{\frac{N}{\pi \prod_{i=1} J_o(\beta_i)}} \right] \frac{\alpha_n \theta_{DL}}{\sin \theta_{UL}} \tag{B-4}$$

where

β_i = uplink modulation indices of subcarriers

θ_{UL} = uplink pseudo-random noise modulation index

θ_{DL} = strong signal downlink pseudo-random noise modulation index

B_L = bandwidth of limiter in receiver IF

$$\alpha_s^2 = \frac{[SNR]_i}{\frac{4}{\pi} + [SNR]_i} \text{ (limiter signal suppression factor)} \tag{B-5}$$

$$\alpha_n^2 = \frac{1}{1+2[SNR]_i} \text{ (limiter noise suppression factor)} \tag{B-6}$$

$[SNR]_i$ = signal-to-noise ratio at limiter input.

The effective downlink pseudo-random noise index is simply

$$\theta'_{DL} = \alpha_s \theta_{DL} \qquad \text{(B-7)}$$

Using these equations, the losses due to the direct turnaround effects can be calculated to permit a direct comparison with the regenerated code case. The results of these comparisons are given in Table 2.9 of Volume 4. The table shows the maximum communication distance for each case with the low-gain antenna and the performance margins at the end of a six-month orbital mission with the high- and medium-gain antennas. There is very little to choose between the approaches in terms of communication distance, thus justifying the use of direct turnaround on the basis of its relative simplicity.

3. PHASE LOCK PARAMETERS

The following paragraphs develop the equations defining the phase locked loops and define the specific parameters for the spacecraft and ground receivers required to support the Voyager orbital mission.

A block diagram of a basic phase lock loop is shown below in Figure B-1.

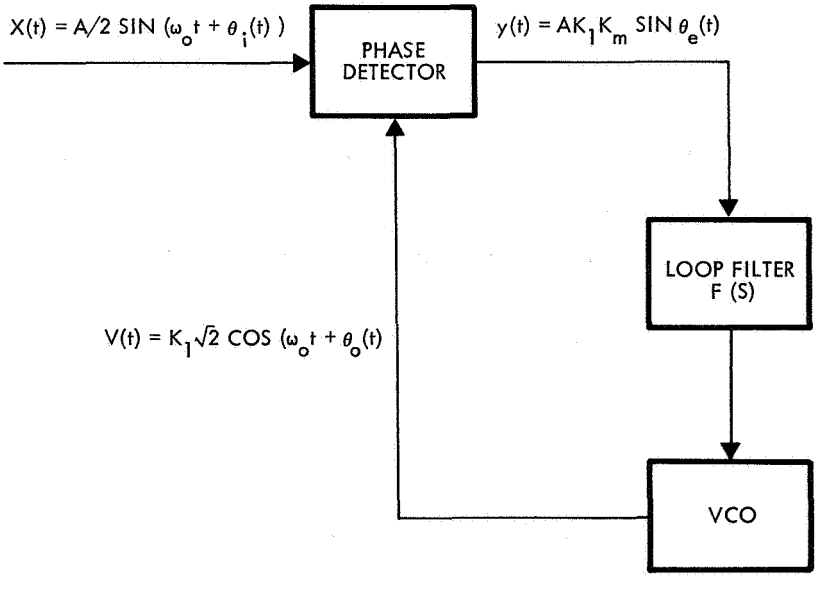


Figure B-1. Block Diagram of Basic Phase Lock Loop

The input to the loop is assumed to be a sinusoid of the form

$$X(t) = A\sqrt{2} \sin (\omega_o t + \theta_i(t)) \tag{B-8}$$

where

A^2 = power of X(t)

ω_o = frequency of VCO with input shorted

$\theta_i(t)$ = the input signal phase process.

The input signal phase process normally consists of an information term due to modulation and a term due to doppler shift in the received signal. The incoming signal is multiplied by the VCO output.

$$V(t) = K_1\sqrt{2} \cos \left[\omega_o t + \theta_o(t)\right] \tag{B-9}$$

The term $\theta_o(t)$ is the loop estimate of $\theta_i(t)$, and K_1 is the rms output of the VCO. The result of this multiplication, if perfect, would be

$$y_1(t) = AK_1 \left\{ \sin \left[\theta_i(t) - \theta_o(t)\right] + \sin \left[2\omega_o t + \theta_i(t) + \theta_o(t)\right]\right\} \tag{B-10}$$

The multiplication is generally accomplished, however, by a device unable to respond to the double frequency term. Also, the multiplying device has some gain, K_m, and so the actual output of the phase detector is:

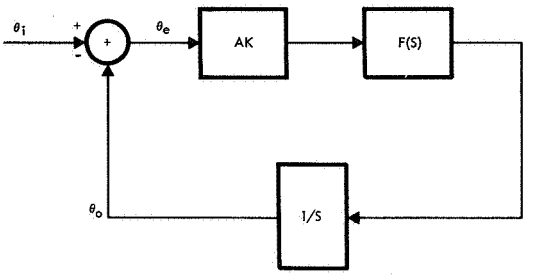
$$y(t) = AK_1K_m \sin \theta_e(t) \tag{B-11}$$

where

$$\theta_e(t) = \theta_i(t) - \theta_o(t) \tag{B-12}$$

is called the phase error.

As is often done, [1, 2] the block diagram of Figure B-1 is redrawn in terms of phase variables in Figure B-2 below. The additional assumption is made that the phase error is sufficiently small so that sin $\theta_e \sim \theta_e$



$K = K_m K_1 K_{VCO}$

K_{VCO} IS THE VCO GAIN CONSTANT IN UNITS OF RADIANS PER SEC PER VOLT.

Figure B-2. Basic Phase Lock Loop in Terms of Phase Variables

The output and error transfer functions for the linearized loop above are easily found and are given below:

$$\frac{\theta_o(S)}{\theta_i(S)} = \frac{AKF(S)}{S + AKF(S)} \qquad \text{(B-13)}$$

$$\frac{\theta_e(S)}{\theta_i(S)} = \frac{S}{S + AKF(S)} \qquad \text{(B-14)}$$

Many different types of loop filters have been used in phase-locked loops. One filter in particular has been widely used and is satisfactory for most applications. This filter is the second-order loop passive filter. As the name implies, use of this filter gives rise to a second-order loop. The passive filter and its transfer characteristics are shown below in Figure B-3.

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[1] Robert C. Tausworthe, "Theory and Practical Design of Phase-Locked Receivers, Volume 1," Technical Report No. 32-819, Jet Propulsion Laboratory, 15 February 1966.

[2] Floyd G. Gardner, and Steven S. Kent, "Theory of Phaselock Techniques as Applied to Aerospace Transponders," George C. Marshall Space Flight Center, National Aeronautics and Space Administration.

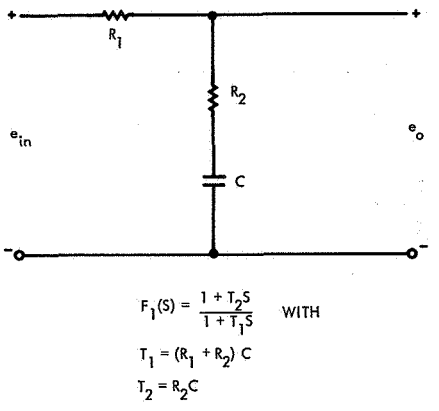

Figure B-3. Passive Filter and Transfer Characteristics

The output and error transfer functions, for a passive filter second-order loop, can then be written as

$$\frac{\theta_o(S)}{\theta_i(S)} = H(S) = \frac{S\omega_n(2\xi - \omega_n/AK) + \omega_n^2}{S^2 + 2\xi\omega_n S + \omega_n^2} \qquad \text{(B-15)}$$

$$\frac{\theta_e(S)}{\theta_i(S)} = 1 - H(S) = \frac{S(S + \omega_n^2/AK)}{S^2 + 2\xi\omega_n + \omega_n^2} \qquad \text{(B-16)}$$

where

$$\omega_n = \sqrt{\frac{AK}{T_1}} \qquad \text{(B-17)}$$

$$\xi = 1/2 \sqrt{\frac{AK}{T_1}} \left(T_2 + \frac{1}{AK}\right) \qquad \text{(B-18)}$$

The three parameters, AK, T_1, and T_2 completely characterize the loop. Alternately, the three parameters AK, ξ, and ω_n also characterize the loop. Criteria for chosing the three parameters, AK, ξ, and ω_n will now be discussed. The open loop gain, AK, is usually chosen to maintain the

doppler tracking error to an acceptable level. With a doppler input, the input phase, $\theta_i(t)$, can be represented as

$$\theta_i(t) = \phi_o + \Omega_o t \tag{B-19}$$

Taking the Laplace transform

$$\theta_i(S) = \frac{\phi_o}{S} + \frac{\Omega_o}{S^2} \tag{B-20}$$

By the final-value theorem of Laplace transform theory

$$\lim_{t \to \infty} f(t) = \lim_{S \to 0} SF(S) \tag{B-21}$$

So

$$\lim_{t \to \infty} \theta_e(t) = \lim_{S \to 0} S\,\theta_i(S) \left[\frac{e(S)}{i(S)} \right] = \frac{o}{AK} \tag{B-22}$$

$$= \frac{o}{AK}$$

Since it is desired to maintain the doppler tracking error to less than approximately 0.1 radian

$$AK = 10\Omega_o \tag{B-23}$$

The damping constant, ξ, will be assumed equal to $1/2\sqrt{2}$. This is the most widely used value of ξ and, as is well known, gives the step phase response with the minimum mean square error.[3] The last parameter, ω_n, is determined by the loop noise bandwidth which is defined below.

---

[3] Benn D. Martin, "The Pioneer IV Lunar Probe: A Minimum-Power FM/PM System Design," Technical Report No. 32-215, Jet Propulsion Laboratory.

$$2B_L = \frac{1}{2\pi} \int_{-\infty}^{+\infty} \left| H(j\omega) \right|^2 d\omega \qquad \text{(B-24)}$$

For the second-order loop with the passive filter[4]

$$2B_L = 1/2w_n \left(2\xi + \frac{1}{2\xi}\right) \qquad \text{(B-25)}$$

with $\xi = 1/2\sqrt{2}$

$$2B_L = 1.06\,\omega_n \qquad \text{(B-26)}$$

where $2B_L$ has the dimensions of Hertz despite the fact that the dimensions of ω_n are in radians per second. The phase error for a doppler rate step input (frequency ramp) with a second-order loop is shown below. The result is true for the active case as well as the passive filter case. The only assumption is that the open loop gain, AK, is much greater than the loop natural frequency, ω_n. This condition is easily satisfied. Only the significant terms in the expression for $\theta_e(t)$ are shown below.[5]

$$\theta_e(t) = \frac{\Delta\omega t}{AK} + \frac{\Delta\omega}{2\omega_n} \qquad \text{(B-27)}$$

where $\Delta\omega$ is the doppler rate in radians per second. The first term in the expression for $\theta_e(t)$ is just the error due to the doppler. This is true because for a frequency ramp input $\Delta\omega t = \Delta\omega$.

So the first term in the expression for $\theta_e(t)$ is $\Delta\omega/AK$, which from Equation (B-22) is just the tracking error due to doppler. The second term in the expression for $\theta_e(t)$ will be denoted by ϕ_{DR}

[4]Floyd G. Gardner, and Steven S. Kent, op. cit., page 4-4.
[5]Ibid., page 5-8.

so

$$\phi_{DR} = \frac{\Delta\omega}{\omega_n^2} \tag{B-28}$$

$$= \frac{1.12\,\Delta\omega}{(2B_L)^2} \tag{B-29}$$

The loop noise bandwidth, $2B_L$, will be chosen so that the maximum tracking error due to a doppler rate input will be about 0.1 radian.

The doppler on the uplink and downlink is given below. The doppler on the uplink is just given as

$$f_u = \frac{v}{c} f_c \tag{B-30}$$

while for the downlink (two-way doppler)

$$f_d = \frac{240}{221} \frac{2\frac{v}{c}}{1+\frac{v}{c}} f_c \tag{B-31}$$

where

f_u = uplink doppler in Hz

f_d = downlink doppler in Hz

f_c = uplink transmitter frequency, 2115 mHz

240/221 = frequency ratio between the coherent downlink carrier and the uplink carrier.[6]

[6]Phase 1A, Task B, Final Technical Report, Voyager Spacecraft, Volume 2, Preferred Design: Subsystems; 17 January 1966.

The doppler rate is just the time derivitive of the doppler, so

$$f_u = \frac{a}{c} f_c \tag{B-32}$$

$$f_d \simeq \frac{240}{221} 2\frac{a}{c} f_c \tag{B-33}$$

The maximum vehicle acceleration, after injection into interplanetary cruise, for the 1973 launch was estimated to be no more than 2.5 meters per second. The maximum doppler rates for the uplink and downlink are therefore given as

$$\dot{f}_u = 17.6 \text{ Hz/sec} \tag{B-34}$$

$$\dot{f}_d = 39.3 \text{ Hz/sec} \tag{B-35}$$

Using Equation (B-29) and setting ϕ_{DR}, the maximum tracking error due a doppler rate, equal to 0.12 radian, the required carrier loop noise bandwidths are found and presented below in Table B-4.

Table B-4. Required Carrier Loop Noise Bandwidths for 0.12 Radar Doppler Tracking Error

	Required Loop Noise Bandwidths, Hz
Uplink	32
Downlink	48

It will now be shown that a sufficiently large loop gain can be obtained to limit the tracking error due to doppler to 0.1 radian. From Equation (B-23), the required open gain, AK, is given as $AK = 10\Omega_o$

where

Ω_o = doppler frequency.

The maximum expected vehicle velocity is about 20 km/sec. Since the uplink frequency is 2115 mHz, the doppler frequency is f_{DU} = 141 kHz. The required open loop gain, AK, is then 1.4×10^6 Hz, which is certainly obtainable.

One further point deserves discussion. As the open loop gain increases, the loop noise bandwidth also increases. Since an increase in the input signal-to-noise ratio reduces the effect of limiter signal suppression, the open loop gain increases with increasing input signal-to-noise ratio. Therefore, the carrier loop noise bandwidth increases with increasing signal-to-noise ratio. A simplified block diagram of the vehicle carrier tracking loop is shown in Figure B-4.

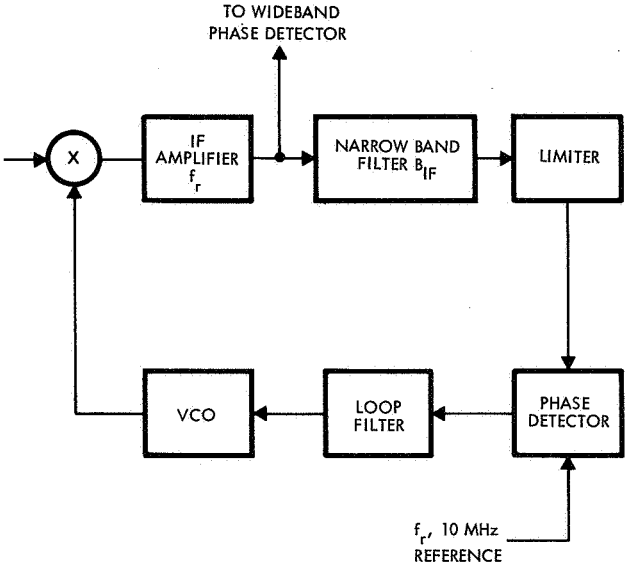

Figure B-4. Simplified Block Diagram of Vehicle Carrier Tracking Loop

The bandwidth, B_{IF}, of the IF filter should be made as narrow as possible in order to minimize the effect of limiter suppression and for easier implementation of the loop lock indicator. The bandwidth must be wide enough, though, so that the loop transfer function is not influenced by the IF filter characteristics. Also, since it is planned to demodulate commands using the narrow band phase detector, the IF bandwidth must be wide enough to pass the command subcarriers. As a reasonable

compromise, then, the narrow-band IF filter will be assumed to be 2 kHz wide. The carrier tracking loop will be designed so that with a loop noise bandwidth of 32 Hz (the minimum required to sufficiently reduce the tracking error due to doppler rate), the signal-to-noise ratio in a 32-Hz bandwidth will be 6 db. The threshold loop noise bandwidth, $2B_{LO}$, for the above loop will now be calculated. The following formula relates the two loop noise bandwidths.[7]

$$2B_{L1} = 2B_{L2} \frac{1}{3}\left(2\frac{\alpha_1}{\alpha_2} + 1\right) \tag{B-36}$$

where $2B_{L1}$ and $2B_{L2}$ are the two loop noise bandwidths and α_1 and α_2 are the respective limiter signal suppression factors. The above formula is only valid when the damping factor for the $2B_{L2}$ loop is 0.707. The limiter signal suppression factor, α, as is well known, is given as[8]

$$\alpha = \left[\frac{\left(\frac{S}{N}\right)_{IF}}{\frac{4}{\pi} + \left(\frac{S}{N}\right)_{IF}}\right]^{1/2} \tag{B-37}$$

where

$\left(\frac{S}{N}\right)_{IF}$ = signal-to-noise ratio in the IF bandwidth,

For small signal-to-noise ratio in the IF bandwidth

$$\alpha \simeq \left(\frac{\pi}{4}\right)^{1/2} \left(\frac{S}{N}\right)_{IF}^{1/2} \tag{B-38}$$

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[7] Floyd M. Gardner, and Steven S. Kent, op cit., page 6-3.

[8] Ibid., page 6-3.

In the following equations, variables representing a 0-db loop parameter will be subscripted with a zero while variables representing a 6-db loop parameter will be subscripted with a 6.

So

$$\left(\frac{S}{N}\right)_{IF_6} = \left(\frac{S}{2B_{L6}\Phi}\right)\left(\frac{2B_{L6}}{B_{IF}}\right) \tag{B-39}$$

$$= 4\,\frac{2B_{L6}}{B_{IF}} \tag{B-40}$$

and

$$\left(\frac{S}{N}\right)_{IF_0} = \left(\frac{S}{2B_L\,\Phi}\right)\left(\frac{2B_{L0}}{B_{IF}}\right) \tag{B-41}$$

$$= \frac{2B_{L0}}{B_{IF}} \tag{B-42}$$

Using Equation (B-38)

$$\frac{\alpha_0}{\alpha_6} = \frac{1}{2}\left(\frac{2B_{L0}}{2B_{L6}}\right)^{1/2} \tag{B-43}$$

Substituting in Equation (B-36) and simplifying,

$$9\left(\frac{2B_{L0}}{2B_{L6}}\right)^{1/2} - 7\left(\frac{2B_{L0}}{2B_{L6}}\right) + 1 = 0 \tag{B-44}$$

Solving

$$\frac{2B_{L0}}{2B_{L6}} = 0.59 \tag{B-45}$$

or

$$2B_{L0} = 19 \text{ Hz} \simeq 20 \text{ Hz} \tag{B-46}$$

Since the carrier power requirement is a signal-to-noise ratio of 6 db in 32 Hz, an equivalent requirement is 8 db in 20 Hz or 8 db in $2B_{L0} = 20$ Hz.

The expanded carrier loop noise bandwidths at encounter and encounter plus six months will now be found.

First the limiter signal suppression factor, α_6, for the 6-db loop must be found. From Equation (B-40)

$$\left(\frac{S}{N}\right)_{IF_6} = 4 \frac{2B_{L6}}{B_{IF}} \tag{B-47}$$

$$= 0.064 \text{ (-11.9 db)} \tag{B-48}$$

Since

$$\alpha_6 = \left[\frac{\left(\frac{S}{N}\right)_{IF_6}}{\frac{4}{\pi} + \left(\frac{S}{N}\right)_{IF_6}} \right]^{1/2} \tag{B-49}$$

$$\alpha_6 = 0.22 \tag{B-50}$$

It is assumed that the vehicle omnidirectional antenna and the ground 210-foot antenna with the 100-kw transmitter are used. The received power-to-noise density ratios at encounter and encounter plus six months are presented below in Table B-5.

Table B-5. Received Power-to-Noise Density Ratios

	R, 10^6 K_m	Received Power-to-Noise Density db x Hz
Encounter	190.7	36.5
Encounter + six months	384	30.5

The loop noise bandwidth expansion will be calculated both for the cases in which there is an uplink subcarrier and for the case in which there is no uplink subcarrier. The only effect of a subcarrier is to reduce the carrier power. This reduction in carrier power effectively causes a further reduction in the signal suppression factor. The ranging and command subcarriers will never be on simultaneously. The loss in carrier power due to either the commands subcarrier or ranging subcarrier being on is 3.2 or 3.0 db, respectively. The calculations will be done for a 3.2-db carrier modulation loss which corresponds to an additional signal voltage reduction of 1.45. From Equations (B-40), (B-43), and (B-45), the limiter suppression factors and loop noise bandwidths are found. Table B-6 summarizes the results for the no subcarrier case while Table B-7 summarizes the results for the command mode case.

Table B-6. Vehicle Loop Noise Bandwidth Expansion with NO Subcarriers

	$\left(\frac{S}{N}\right)_{IF}$, db	α	$2B_L/2B_{L6}$	$2B_L$, Hz
Encounter	3.5	0.80	2.75	88
Encounter + six months	-2.5	0.55	2.0	64

Table B-7. Vehicle Loop Noise Bandwidth Expansion with Command Subcarrier

	$\left(\frac{S}{N}\right)_{IF}$, db	α	α/ML^*	$2B_L/2B_{L6}$	$2B_L$, Hz
Encounter	3.5	0.80	0.55	2.0	64
Encounter + six months	-2.5	0.55	0.38	1.5	48

*ML = 1.45 and is the signal suppression factor due to carrier modulation loss.

DSIF Carrier Tracking Loop Parameters. The DSIF carrier tracking loop has the capability to operate with any of four different loop filters. Table B-8 lists the strong signal and threshold loop noise bandwidths for the carrier tracking loop, for each of the loop filters.[9]

Table B-8. DSIF Threshold Loop Noise Bandwidth

Threshold Loop Noise Bandwidth ($2B_{L0}$), Hz	Strong Signal Noise Bandwidth, Hz
5	50
12	120
48	255
152	500

The threshold loop noise bandwidth is the bandwidth with a 0-db signal-to-noise ratio in the loop bandwidth. The required loop noise bandwidth for the downlink is given as 48 Hz from Table B-4. It is desired to use the loop filter that provides a 48-Hz loop bandwidth with the minimum signal power-to-noise density ratio. The variation of loop noise

[9]E. C. Gatz, and R. B. Hartley, "Planned Capabilities of the DSN for Voyager 1973," Engineering Planning Document No. 283, Revision 2, 1 January 1967, page 13.

bandwidth with signal-to-noise ratio for the DSIF carrier tracking loop is plotted in a DSIF specification.[10]

From the DSIF specification, a signal with 15 db more power than the threshold signal is required to increase the $2B_{L0}$ = 12 Hz bandwidth to $2B_L$ = 48 Hz. A 0-db signal-to-noise ratio in the $2B_{L0}$ = 48 Hz loop, though, requires 15-6 = 9 db less signal-to-noise ratio than 15 db in $2B_{L0}$ = 12 Hz. Even 6 db in $2B_{L0}$ = 48 db requires 3 db less signal-to-noise density ratio than 15 db in $2B_{L0}$ in 12 Hz. Therefore, the carrier power requirement will be a 6-db signal-to-noise ratio in $2B_{L0}$ = 48 Hz. With 6 db in $2B_{L0}$ = 48 Hz, the loop noise bandwidth expands to 80 Hz.

[10]Spacecraft/DSIF/GOE Interface Specification PC-2.00 through PC-2.04, National Aeronautics and Space Administration, Ames Research Center, Moffett Field, California, Document No. PC-2.01.

APPENDIX C

ANTENNA DRIVE TRADEOFF STUDIES

The major antenna drive elements which were considered in tradeoff studies were the gimbal system, the drive mechanism, and the prime mover.

1. GIMBAL SCHEMES

Two gimbal schemes were considered: 1) the standard cross gimbal, and 2) the differential gimbal. Figure C-1 gives the tradeoff considerations for the two schemes. In this application, it is obvious that although the differential gimbal has its applications (for example, concentric drives), its complexity and size make it less attractive. On the other hand, the cross gimbal makes for a rugged, and compact package.

2. DRIVE MECHANISM

Six drive mechanism schemes were considered: 1) the wabble gear, 2) the harmonic drive, 3) the spur gear drive, 4) the linear ball screw drive, 5) the worm gear, and 6) the direct drive. Table C-1 compares these schemes.

An important requirement for the drive mechanism is that it be adaptable to a noncontacting rotary RF joint. This is necessary in order to maintain low transmission losses. With these rotary joints the VSWR can be maintained less than 1.2:1, with an insertion loss of 1.0 ±0.1 decibel, including mismatch loss, in the antenna cable. Another requirement is that the drive mechanism be compatible with the gimbal scheme.

The wabble gear drive mechanism has been used successfully for the OPEP and solar array drives for the OGO spacecraft. Its major

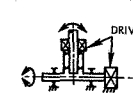
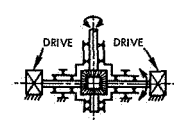
GIMBAL ARRANGEMENTS	TRADEOFFS		
	RELIABILITY		COMPLEXITY
	NUMBER OF CRITICAL PARTS	PERFORMANCE CHARACTERISTICS	
STANDARD GROSS GIMBAL 	BEARINGS: 4 GEARS: 0 STRUCTURAL: 3	MOVEMENT ABOUT ANY ONE AXIS REQUIRES INPUT FROM ONE DRIVE ONLY. FAILURE OF ONE CRITICAL PART CAUSES FAILURE OF ONE AXIS ONLY	MINIMUM COMPLEXITY. SIMPLE TO PACKAGE, MANUFACTURE, AND ASSEMBLE. MINIMUM MANUFACTURING COST
DIFFERENTIAL GIMBAL 	BEARINGS: 10 GEARS: 4 STRUCTURAL: 3	MOVEMENT ABOUT ANY ONE AXIS REQUIRES THAT BOTH DRIVES OPERATE SIMULTANEOUSLY. FAILURE OF ONE CRITICAL PART CAUSES FAILURE OF BOTH AXES	HIGHLY COMPLEX. DIFFICULT TO PACKAGE, MANUFACTURE, AND ASSEMBLE. HIGH MANUFACTURING COST

Figure C-1. Gimbal Tradeoff Summary

Table C-1. Sealed Drive Tradeoff Summary*

Sealed Drive Candidates	Performance	No. of Gears Based on 100:1 Reduction	Number of Rotating Seals	Size and Weight	Packaging
Wabble Gear Calculated Reliability Single axis: 0.9933 Two axis: 0.986	High efficiency, high torque transmission, good accuracy	Gears: 2	None Uses bellows and static "O" ring or hermetic seals	Small and light	Internal design moderately simple, packages extremely well with gimbal.
Harmonic Drive	High efficiency, Moderate torque transmission, good accuracy	Gears: 2	None Uses thin flexible metal tube which is exposed to space. High speed elements are sealed.	Small and light	Internal design moderately simple, very difficult to package with gimbal, requires additional gears and bearings.
Spur Gear Drive	Moderate efficiency, high torque transmission, good accuracy	Gears: 8 (Based on 4:1 reduction per gear mesh)	Two sets of seals	Small and light	Internal design moderately simple, more parts required than the above, can be designed to package well with gimbal
Linear Ball Screw Drive	Moderate to high efficiency, depending on number of gears used. High load transmission, good accuracy. Some losses do occur due to differential gas pressure acting on bellows	Gears: 2 to 8 plus ball screw assembly	None Uses bellows and static "O" ring or hermetic seals	Large and heavy due to large stroke required to obtain gimbal travel	Internal design could range from moderately simple to complex, will not package well with gimbal, requires long stroke to achieve gimbal travel, not suited to this application
Worm Gear	Low to moderate efficiency, high torque transmission, good accuracy	Gears: 2 (gears have large sliding surfaces)	Two shaft seals	Small and light	Internal design moderately simple, can be designed to package well with gimbal
Direct Drive	Highest efficiency, high torque transmission, good accuracy	No gears	Two sets of seals	Small size and weight for drive; motor diameter prohibitive due to torque requirements	Internal design may be simple, package can be designed for gimbal

*Sealed Drive Tradeoff Summary shows that major advantages of the wabble gear drive are that fast moving surfaces are sealed from the vacuum environment and it forms a compact gimbal package that can easily include a radio frequency joint.

advantages are that 1) fast moving surfaces are sealed from the vacuum environment, and 2) it makes a compact gimbal package with the RF joint easily included.

The harmonic drive, developed by United Shoe Machinery Co., also has its fast moving surfaces sealed from the vacuum environment. However, the incorporation of the rotary RF joint in the gimbal scheme is not easily accomplished.

The spur gear drive and the direct drive need dynamic seals to protect the motor, bearing, and other moving parts from the environment. The direct drive is usually used with a slow-speed, high-torque device, such as a DC motor.

The linear ball screw is normally used when rotary motion is converted to linear motion. In this application, it offers no real advantages, because of the long stroke which would be required and the linear-to-rotary conversion mechanism needed.

The worm gear has low to moderate efficiency. This has the advantage that the worm gear can be designed so that it cannot be back-driven; this would be useful during engine firing. Its main disadvantage is that its gears have large sliding surfaces which cause rapid wear and it requires shaft seals to protect the moving parts from the space environment. Failure of the seal due to wear or to breakdown will cause loss of lubrication which will cause galling or welding the worm gears, and deposition of oil vapor on delicate parts and lenses of other spacecraft components.

3. PRIME MOVER

Three prime movers are considered in this application: 1) DC torque motor, 2) stepper motor, and 3) AC servo motor. High reliability, minimum weight, and low electromagnetic interference (RFI) are standard objectives in spacecraft design. An additional requirement of the Voyager spacecraft is that nonmagnetic material be used except when no other alternatives are available.

Table C-2 presents the tradeoff analysis for the prime movers. The DC torque motor has the disadvantage of a high permanent magnet field, high RFI due to commutator sparking, brush wear with high currents, and moderate weight and size.

Table C-2. Prime Mover Tradeoff Summary*

	Performance	Life and Reliability	Size and Weight	RFI	Magnetic Field	Comments
DC Torque Motor	High torque to inertia ratio, high coupling stiffness, fast response	May be short-lived because of brush wear, otherwise high reliability	Moderate size and weight due to lack of gearing to load	High unless filtered	Large, stationary magnetic field	Constant torque required out of motor to hold load
Stepper Motor	Constant speed, high resolution, fast response	Not as long life as AC servo motor	Moderate to large size due to slow rotor speed, inertial loads	No RFI generated by motor, driver pulsed output can be troublesome	Uses permanent magnet motor	This is a digital device and does not require D/A conversion in a computer system. Needs complex electronics for driver
AC Servo Motor	High-speed, low-torque device, slow response due to high gearing ratio to load	Long life, rugged and reliable	Small size and light weight	No RFI generated by motor	No stationary magnetic field	High speed components need to be sealed and pressurized

*Prime mover tradeoff summary shows that the AC servo motor is the best choice for the antenna assemblies.

The stepper motor would require complex electronic circuitry. Also, the weight and the size penalty would negate its other advantages.

The AC servo motor offers the best choice as prime mover for the antenna drive assemblies. Furthermore, it has been used in control systems for a long time, and much engineering experience and background has been accumulated so as to make maximum use of its advantages.

4. SHAFT POSITION TRANSDUCERS

Shaft position transducers are required to serve two functions, first to provide control system feedback and, second to provide telemetering feedback. These two functions should be electrically isolated from each other. Ideally, the transducers are coupled directly to the output shaft.

Both analog and digital devices were considered for this application. While analog devices generally give an absolute output for any given angular position, their inaccuracy results from the effective deviations of the straight line characteristic of the input-output curve due to various factors including environmental conditions, inherent errors and loading effects. On the other hand, the digital transducer or shaft position encoder presents a "step-like" input-output curve where, instead of a one-to-one correspondence between input and output, the output is constant for a small range of input values. Making the digital increments smaller than the inaccuracy, displacement and nonlinearity shifts of the corresponding analog curve results in an inherently more accurate system. The reason for this improvement lies in the binary representation of the input quantity. Although each digit is in essence affected by analog errors, the incorporation of more than one binary digit to describe the input results in an exponential decrease of the otherwise overall analog error.

Two types of analog devices, the potentiometer and the resolver, were considered for possible use. Although potentiometers may be obtained which will yield the required resolution and accuracy they depend on brushes for electrical contact between the stationary and rotating elements. Brushes are susceptible to shock, vibration and

wear. Also, the requirements for long life, high resolution, and continuous rotation dictate the use of a film type potentiometer, but this type nominally has an electrical travel of only 350 degrees. Thus, it appears that a potentiometer would not fulfill all the requirements.

Resolvers eliminate the need for mechanical contact between the stationary and rotating members by depending on magnetic coupling instead. The resolver produces two outputs which are sine and cosine functions of the shaft angular position. Both outputs are needed however, to provide unambiguous position information. Because of the form of the resolver signals complex electronic conditioning circuitry is required to make the feedback information compatible with commanded position inputs (probably digital) and tracking error signals (DC).

Shaft position encoders are basically of four types. These include: 1) brush in which readout is effected conductively through brushes making contact with a segmented disc, 2) magnetic in which readout is effected magnetically, 3) capacitive in which readout is effected electrostatically, and 4) optical-photoelectric in which readout is effected by photoelectric means. These types can be further divided into devices in which successive increments of position are indistinguishable and must be counted, and devices in which successive positions are uniquely coded so that absolute position information can be determined directly. Since the resolution required is 0.01 degree or better, the direct reading encoders must produce 16 bits of information, i.e., 16 coded tracks are required. These encoders are subject to errors that arise from incorrect relative positioning of multiple tracks, from optics, brushes or magnetic or capacitive pickoffs to read these multiple tracks, and from radial misalignment of an indexing assembly. Moreover, the brush devices have multiple brush problems, the photoelectric devices require light sources of questionable long life, the capacitive devices are very sensitive to noise, and the magnetic devices produce rotating permanent magnet fields.

The incremental encoder represents the simplest type of encoder usually consisting of a rotating disk having a single track of equally spaced

segments and a suitable sensing member. The data is derived in increments and must be accumulated in external circuitry to represent shaft position. The direction of shaft rotation is obtained by using the output of a second pickoff displaced in phase 90 degrees from the primary output. By operating logically on the outputs of the two pickoffs direction of rotation can be determined. A disadvantage of using incremental encoders for position determination is that errors generated by noise transients, power failure and other sources are accumulated. With the addition of reference points and another pickoff to the encoder and careful design of the associated electronic circuitry these errors may be minimized. Rate information may be obtained because the pulse rate generated is a function of shaft speed. High accuracy rate data can be obtained by counting the number of encoder output pulses as a function of time.

In summary the magnetic incremental type position encoder is recommended for the following reasons:

- There is no mechanical contact between the rotating and stationary members
- The use of two pickoffs on a single track eliminates the sources of error inherent in multiple track encoders
- The external circuitry required is quite simple even when compared to direct reading encoders. Although direct reading encoders provide a unique output for each discrete shaft position, the output is usually in a cyclic code which must be converted to another binary form to be compatible with other signals.
- Physical configuration is readily adaptable to mounting on hollow shafts
- The required resolution may be obtained when the encoder is coupled directly to the output shaft

- The extremely simple construction and absence of mechanical contact means high reliability and long life
- Rate information is easily obtained if required
- The incremental encoder is readily adaptable to control systems where the commanded input is representative of either absolute position or an incremental change in position.

5. ROTARY JOINT

The RF transmission path is required to traverse two axes of rotation in the high gain antenna assembly. Three methods of providing the required relative motion across the axes were studied. These were 1) cable wrapup, 2) contacting rotary joints, and 3) noncontacting rotary joints. The cable wrapup was considered the least desirable due to the bulk and weight resulting from the number of turns required. Spring tension exerted on the actuator mechanism and fatigue of the coaxial cable were also considered as a reliability factor.

Flexible cable would be used for this case, but consideration of its becoming a rigid element under low temperature conditions if the cable heater failed, necessitated a layout on the basis of its behavior as a rigid coil structure. This would require a bobbin and minimum of six turns per axis on approximately a 6-inch diameter with additional radial clearance for growth during rotary motions, causing unwinding of the coil. Such an arrangement would weigh approximately three times that of the noncontacting rotary joint arrangement selected and would have the additional negative factors of noise during flexure, increased electrical losses due to the additional cable lengths involved, and restriction of angular rotation in one axis.

The contacting type rotary joint was eliminated due to problems associated with providing reliable electrical continuity without contact welding in a space environment. The noncontacting type is recommended as being the simplest, most reliable, and also the lightest in weight. By utilizing the bearing structure integral with the actuator geometry,

and so arranging the actuator shafting to accommodate the required hardware, it is possible to design the rotary joints into the actuator assembly so that they became an integral part of that assembly, using its bearing system for joint alignment. For this reason it is not mechanically correct to discuss these joints as separate items, from the actuator. Incorporation of the rotary joints into the actuator assembly adds approximately 0.38 pound each to the overall weight of the actuator.

6. MOTOR DRIVE POWER

Tradeoffs were made in the area of motor drive power generation. Primarily, two techniques were investigated to determine advantages of each approach from the standpoint of efficiency and parts count. Employing external AC drive power and commutating the conversion efficiency of the output stages which to a great extent determines subsystem efficiency proved to be a better selection from the standpoint of driver efficiency and total parts count.

APPENDIX D

COMMAND BIT SYNCHRONIZER

1. DETECTION

A PCM bit stream that has been passed through a noisy communication channel may be represented as[1]

$$y(t) = \sum_i f_i(t - iT + t_o) + n(t) \qquad \text{(D-1)}$$

where

$y(t)$ = the received signal plus noise

$f_i(t)$ = either one of two preselected bit waveforms $S_1(t)$ or $S_2(t)$

T = the bit period

t_o = an unknown time delay ($0 \leq t_o \leq T$).

The additive noise may usually be assumed to be Gaussian. The bit waveforms $S_1(t)$ and $S_2(t)$ are preferably selected for optimum signal design performance[2] corresponding to a regular simplex code, for which $S_1(t) = -S_2(t)$. This is the case for standard NRZ (C, M, or S) and split-phase telemetry formats; however, this is not true for RZ signals, which instead correspond to an orthogonal code and thereby must yield 3 db degradation in theoretical performance.

The function of a bit synchronizer is to coherently detect the received signal $y(t)$, i.e., to reconstruct the original PCM data stream [a "0" corresponds to transmition of $S_1(t)$ waveform and a "1" corresponds to the transmission of $S_2(t)$ waveform]. In performing this function, the bit synchronizer may be considered to perform two operations:

1) Estimating (or locking onto) the unknown time delay t_o

2) Detecting (or deciding) whether signal $S_1(t)$ or $S_2(t)$ was transmitting each bit period.

Assuming that the first operation can be ideally accomplished (i.e., with zero error or with no phase jitter in the local bit rate time reference generated by the bit synchronizer system), the calculation of the resulting bit error rate (BER) for the second function can be easily accomplished. When the additive noise has a flat spectral density (white noise), the error probability is given by[3] (as a function of signal-to-noise ratio λ).

$$P_E(\lambda) = 1 - \phi\left(\sqrt{\frac{1-\gamma}{2}}\right) \tag{D-2}$$

where

$$\phi(x) = \text{cumulative Gaussian distribution} \tag{D-3}$$

$$\phi(x) = \int_{-\infty}^{x} \frac{\ell^{-1/2x2}}{\sqrt{2\pi}}\, dx$$

and

$$\lambda^2 = \frac{\text{signal energy (per bit)}}{\text{noise spectral density}} = \frac{E}{N_o} \tag{D-4}$$

where

λ = the cross correlation coefficient between the two possible bit waveforms $S_1(t)$ and $S_2(t)$.

For the case of either NRZ or split-phase (Manchester) signal codes, the correlation coefficient $\gamma = -1$, so that

$$P_E(\lambda) = 1 - \phi(\lambda) = \phi(-\lambda) \tag{D-5}$$

However, for the case of an RZ code, $\gamma = 0$ and

$$P_E(\lambda) = 1 - \phi(\lambda/\sqrt{2}) = \phi(-\lambda/\sqrt{2}) \tag{D-6}$$

which indicates the inherent 3 db degradation of theoretical performance of an RZ code with respect to an NRZ code. These ideal error rate curves are plotted in Figure D-1.

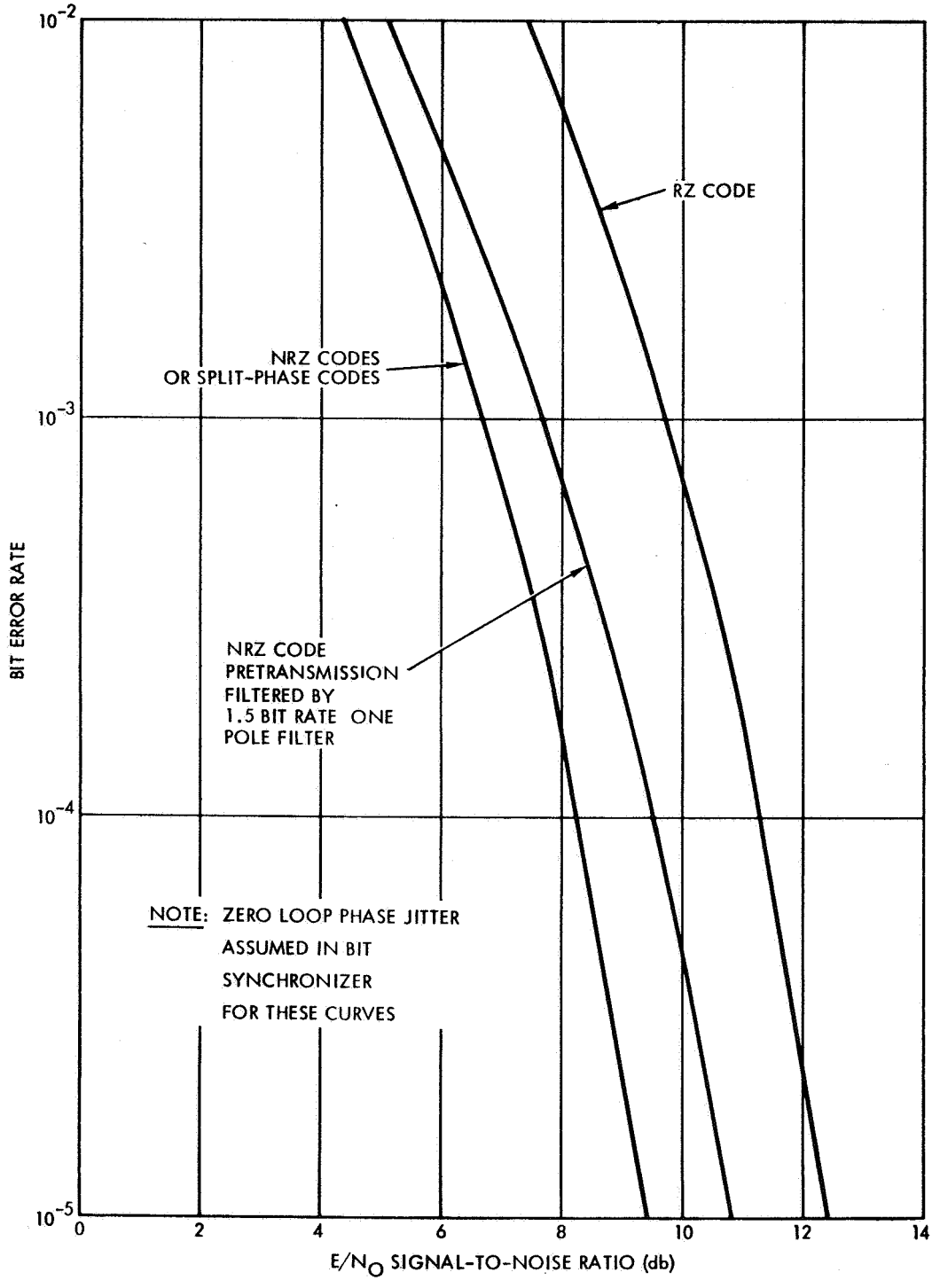


Figure D-1. Ideal Bit Error Rate Curves

In actual practice, of course, a real bit synchronizer system can only approach these ideal performance curves due to imperfect knowledge of the time delay (i. e., a nonzero amount of phase jitter in the locally generated bit rate reference of the bit synchronizer loop) and due to the imperfections of the matched filter detection system (e. g., integrate and dump filter). For example, phase jitter of the VCO, DC offsets and time delays in the integrator and comparator circuits, and imperfect tracking of baseline variations of the input signal all degrade the achievable performance. In addition, the presence of bit rate jitter on the input signal represents an additional uncertainty (or noise component) added to the signal and implies an additional performance degradation. Each contributing cause of degradation may be appropriately analyzed by incorporation of its corresponding random perturbation into the mathematical detection model of the bit synchronizer system.

The theoretical BER curves are unrealistic in that they assume no theoretical loss due to imperfect knowledge of the bit rate clock, which is equivalent to the assumption of a zero bandwidth phase lock tracking loop in the bit synchronizer. A more realistic model is one which the BER is calculated for a given nonzero loop noise bandwidth B_o. This is equivalent to saying that the lock acquisition time (which depends on the loop noise bandwidth) should be kept as a parameter in the theoretical BER curves. When this is done, it can be shown that, for the case of NRZ input data at 50 percent transition density, the theoretical BER is given by

$$P_E = 1 - (1/2)\,\phi(\lambda) - \int_o^\infty \phi\left[\lambda - \frac{1}{\pi}\sqrt{\frac{B_o}{B_r}}\,y\right]\frac{\ell^{-1/2y^2}}{\sqrt{2\pi}}\,dy \qquad \text{(D-7)}$$

where λ^2 is the signal-to-noise ratio and B_r is the bit rate. Hence, an error rate curve can be plotted versus signal-to-noise rate (similar to Figure D-1) with relative loop bandwidth B_o/B_r as a parameter. The actual performance of the bit synchronizer for the same relative loop bandwidth should then be compared with this theoretical limit, to determine the true performance degradations. Note that when the relative loop bandwidth B_o/B_r approach zero, the BER of Equation (D-7) reduces to the previous Equation (D-5) for the case of no assumed loop jitter due to noise.

2. SYSTEM APPROACH

The PCM bit synchronizer must perform the functions of estimating the location of the bit-time period and detecting the binary data present in each bit period (as described in Section 1). The most efficient technique for accomplishing the former function in the presence of noise is to employ methods of automatic phase-lock loop control. The important advantages of phase-lock loop tracking of the bit rate clock relate to the inherent capability for noise rejection by utilizing narrow loop bandwidths. This permits useful operation of the bit synchronizer at extremely small input signal-to-noise ratio if desired, i. e., the minimum threshold signal-to-noise ratio for useful operation may be reduced as desired. Other less attractive techniques for bit-rate clock generation are certainly possible, but these techniques result in less noise suppression capability and tend to exhibit rapidly degrading performance at low signal-to-noise ratio. One typical example is that of zero-crossing detection of a split-phase coded PCM signal as a method of estimating the bit-rate clock. A possible disadvantage of the phase-lock loop method is the rapid increase in acquisition time as the loop bandwidth is reduced to accommodate low signal-to-noise ratio operation; however, at low signal-to-noise ratio, a larger acquisition time is naturally expected because of the greater uncertainty which exists concerning the true location of the bit time period (or phase) and the true bit rate frequency.

Given some type of phase-lock loop to achieve bit-rate clock tracking, the optimum technique for bit data detection is easily determined. It is well known[4, 5, 6] that the optimum detector in the presence of additive Gaussian noise is the matched filter having the frequency transfer function H(jw) given by

$$H(jw) = \frac{S^*(jw)}{G_n(f)} e^{-jwt_1} \qquad \text{(D-8)}$$

where

$S(jw)$ = Fourier transform of the bit waveform to be detected

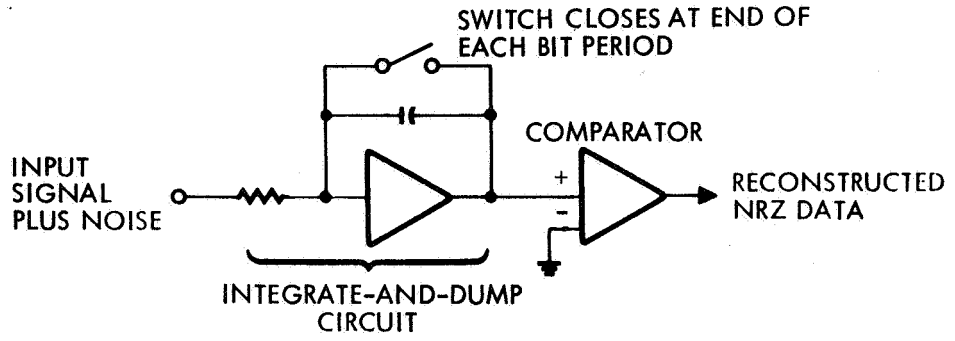
$G_n(f)$ = power spectral density of the independent additive noise.

This matched filter output maximizes the signal-to-noise ratio at time t_1. For the important case where the noise spectrum is flat $G_n(f) = N_o$, the filter impulse response is a time-inverted replica of the signal bit waveform S(t), and furthermore, the filter signal plus noise output at the end of the bit time is proportionally equal to

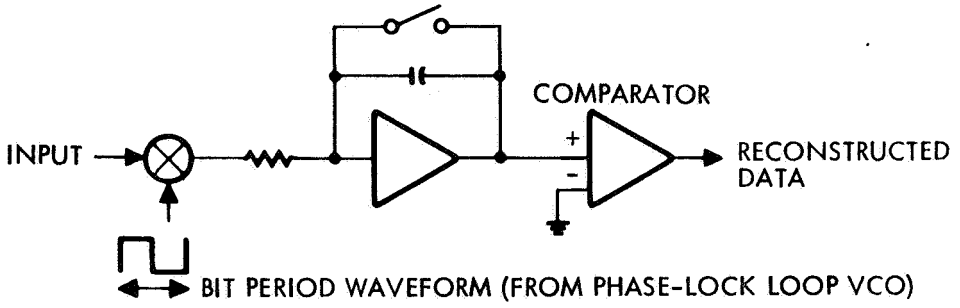
$$\int_o^T S^2(t)\, dt + \int_o^T S(t)\, n(t)\, dt \qquad \text{(signal present)} \qquad \text{(D-9)}$$

The matched filter in this case is called a correlation detector. When the PCM signal format is NRZ, the filter becomes the well-known integrate-and-dump circuit. For split-phase data (Manchester coding) the matched filter consists of an integrate-and-dump circuit preceded by a square wave multiplier at the bit rate frequency. For RZ data the matched filter is an integrate-and-dump circuit, except that the timing is arranged to allow the integration only over the first half of the bit period. These matched filter detection circuits are illustrated in Figure D-2.

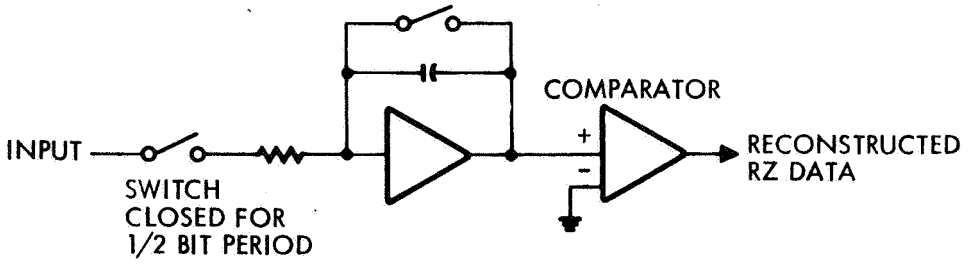
As a result of the above theoretical considerations, the general form of the bit synchronizer system which will be required to optimally reconstruct the PCM data is now clearly indicated: phase-lock loop tracking is needed to generate the bit-rate clock plus some form of integrate-and-dump circuit to perform binary signal detection. One important complication arises: the bit synchronizer phase-lock loop cannot always track the bit rate when provided with modulated input data. This is because there is only a reduced bit rate frequency component present in the input data stream when the transition density is near 50 percent. To overcome this difficulty the data must be demodulated (i.e., removed) in an appropriate manner before being applied to the phase-lock loop. This requirement to restore the bit frequency component, as well as all previously mentioned requirements, is conveniently and effectively satisfied by the system TRW proposes, an I-Q bit synchronizer, or a modified "Costas Synchrolock Demodulator."[7] A description of the I-Q bit synchronizer operation is presented in paragraph 2.2.



(A) NRZ FORMAT



(B) MANCHESTER CODING FORMAT



(C) RZ FORMAT

Figure D-2. Matched Filter Detection for Various PCM Telemetry Formats

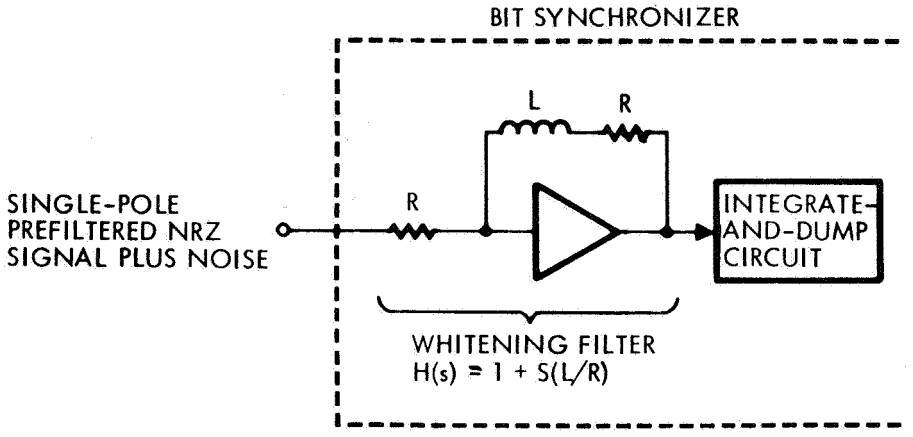
2.1 PREFILTERED CASE

It should be mentioned that the above discussion assumes that the input noise is white and the input signal is undistorted. In the case where there is post transmission filtering of the signal plus noise before application to the bit synchronizer, the matched filter additionally consists of a whitening filter (the inverse of the prefilter).[8] This conclusion is a direct consequence of Equation (D-8). For example, if the prefilter is a simple one-pole low-pass filter, the whitening filter will be as shown in Figure D-3a. This configuration, in combination with the integrate-and-dump circuit, represents the appropriate matched filter for the prefiltered case, as given by Equation (D-8). Note that the theoretical BER is still given by the curves of Figure D-1.

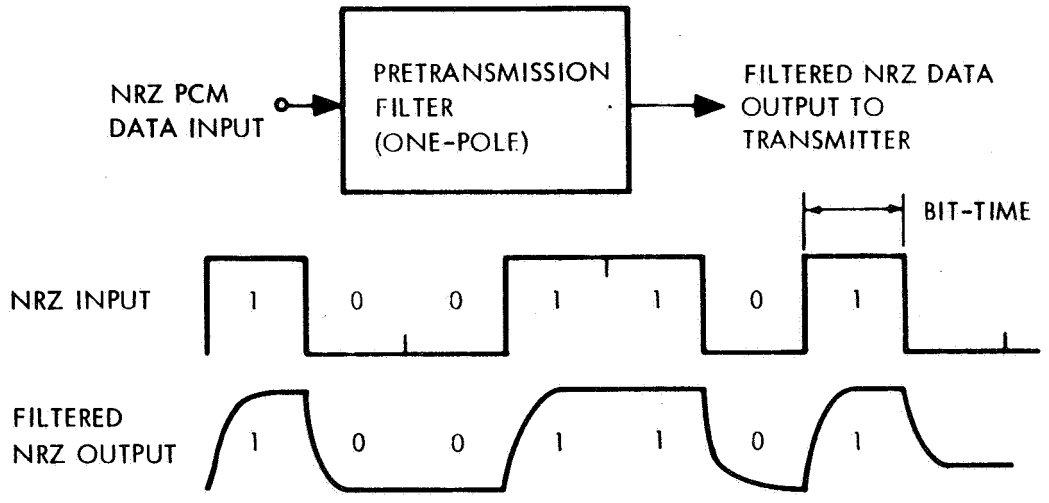
Another possibility is that the PCM data stream in prefiltered before transmission (to conserve link bandwidth). In this case an integrate-and-dump filter is not optimum. For example, if a single-pole pretransmission filter is used having a 3-db bandwidth equal to 1.5 times the bit rate for NRZ data, then Equation (D-8) yields the optimum matched detector filter,

$$H(jw) = \left(\frac{1 - e^{-jwT}}{jw}\right) \cdot \frac{e^{-jw(t_1 - T)}}{1 - jwT/3\pi} \qquad \text{(D-10)}$$

The first expression in parenthesis is the transfer function for an integrate-and-dump circuit, and the second expression represents a time delay $t_1 - T$ and a filter having a pole in the right half plane. Of course, this filter is physically unrealizable by conventional passive filtering techniques. One possibility is to permit the time delay t_1 (at which the matched filter output is sampled) to exceed the bit time T, and to approximate the resulting transfer function by physically realizable filters. This approach tends to be complex and has the disadvantage of increased time delay in the bit synchronizer loop which degrades the loop acquisition properties.[9] When the allowed delay t_1 is constrained to be equal to the bit time, then it can be shown by Wiener filtering theory[5] that the optimum realizable matched filter is the integrate-and-dump filter (this is also true when any n-pole pretransmission filter is used). This approach is commonly used in the design of bit synchronizers.[10]



(a) OPTIMUM MATCHED FILTER FOR SINGLE-POLE POST-TRANSMISSION FILTERED NRZ DATA PLUS NOISE



(b) WAVEFORMS FOR PRETRANSMISSION FILTERED NRZ DATA

Figure D-3. Case of Prefiltered NRZ Signals

Note also that the use of pretransmission filtering causes intersymbol interference in the detection process performed by the bit synchronizer, (due to the presence of data waveform "tails" extending over adjacent bit-time periods due to the pulse-stretching effect of the prefilter). This is illustrated in Figure D-3b. It is possible to compensate approximately for the effect of intersymbol interference by adjusting the decision threshold of the comparator circuit (Figure D-3a) if a transition occurs in any given bit-period;[11] however, the threshold adjustment requires an a priori knowledge of the signal power levels at the integrate-and-dump circuit output. Due to the wide dynamic range of the input signal and signal-to-noise ratio to the bit synchronizer, it is therefore not considered feasible to perform this threshold adjustment to compensate for intersymbol interference.

The theoretical BER curve for the case of pretransmission filtering of NRZ data may be described as follows: Let M be thr transition density and h(t) the unit step response function for the prefilter. If no intersymbol interference compensation is used for the integrate-and-dump detector, then the BER is given by

$$P_E = M\left[1 - \phi(k\lambda)\right] + (1 - M)\left[1 - \phi(\lambda)\right] \qquad \text{(D-11)}$$

where λ and $\phi(\lambda)$ are defined by Equations (D-3) and (D-4) for the unfiltered NRZ data, and

$$k = \frac{\int_0^T \left[2h(t) - 1\right] dt}{\int_0^\infty h(t)\, dt} \qquad \text{(D-12)}$$

For example, if the pretransmission filter is a simple one-pole filter having a 3 db cutoff frequency equal to 1.5 times the bit rate of the NRZ data, then $h(t) = 1 - e^{-3\pi t/T}$ and $k = 0.788$. The BER for this case is plotted in Figure D-1 for $M = 0.5$ versus the average signal-to-noise ratio 0.947λ. Note that the same comment as before applies to this theoretical curve, namely a perfect bit rate phase-lock loop is assumed in the bit synchronizer; a different theoretical curve applies similar to Equation (D-7) when nonzero loop bandwidth is taken into account.

In summary, the theoretical bit error rate curves are directly obtained by methods and mathematical relationships which have been described in this section of the proposal. The curves can take into account the various types PCM signal waveforms which are used, the prefilter which is used as well as the loop phase jitter for the actual loop bandwidth used in the bit synchronizer.

2.2 I-Q BIT SYNCHRONIZER FUNCTIONAL DESCRIPTION

A general block diagram of the proposed I-Q bit synchronizer is shown in Figure D-4. A conceptual description of its operation is given below, and a more detailed functional description of the mechanization and the logic and analog circuitry is presented in paragraph 2.3. The major signal waveforms in the loop are sketched in Figure D-5, assuming a split-phase modulated input signal under the condition where the phase-lock loop has achieved bit-rate sync lock.

The buffer amplifier in Figure D-4 performs conditioning of the received signal plus noise waveform y(t). A whitening filter is provided here, if necessary, for the prefiltered case. Rejection of static and dynamic baseline offsets is accomplished by application of AC coupling and DC restoration techniques; for NRZ-C data, the DC component is also a function of the transition density and AC coupling alone is insufficient. The use of a subcarrier avoids all of these baseline problems. Additionally, automatic gain control (AGC) of the buffer amplifier may be provided to maintain its output signal component constant (this may be a requirement, since the loop gain K is proportional to applied signal level and the loop noise bandwidth is proportional to $K^{1/2}$).

The conditioned signal plus noise is then applied to the I and Q channels of the bit synchronizer loop (Figures D-4 and D-5). The cascaded functional elements in the I channel (switching multiplier, integrate-and-dump circuit, comparator and sample and hold circuit) constitute the exact matched filter detector for split-phase modulated PCM signal, as has been discussed in connection with Equation (D-8). Thus, when the loop is in a locked condition, the I channel output $e_1(t)$ provides the reconstructed data in NRZ form.

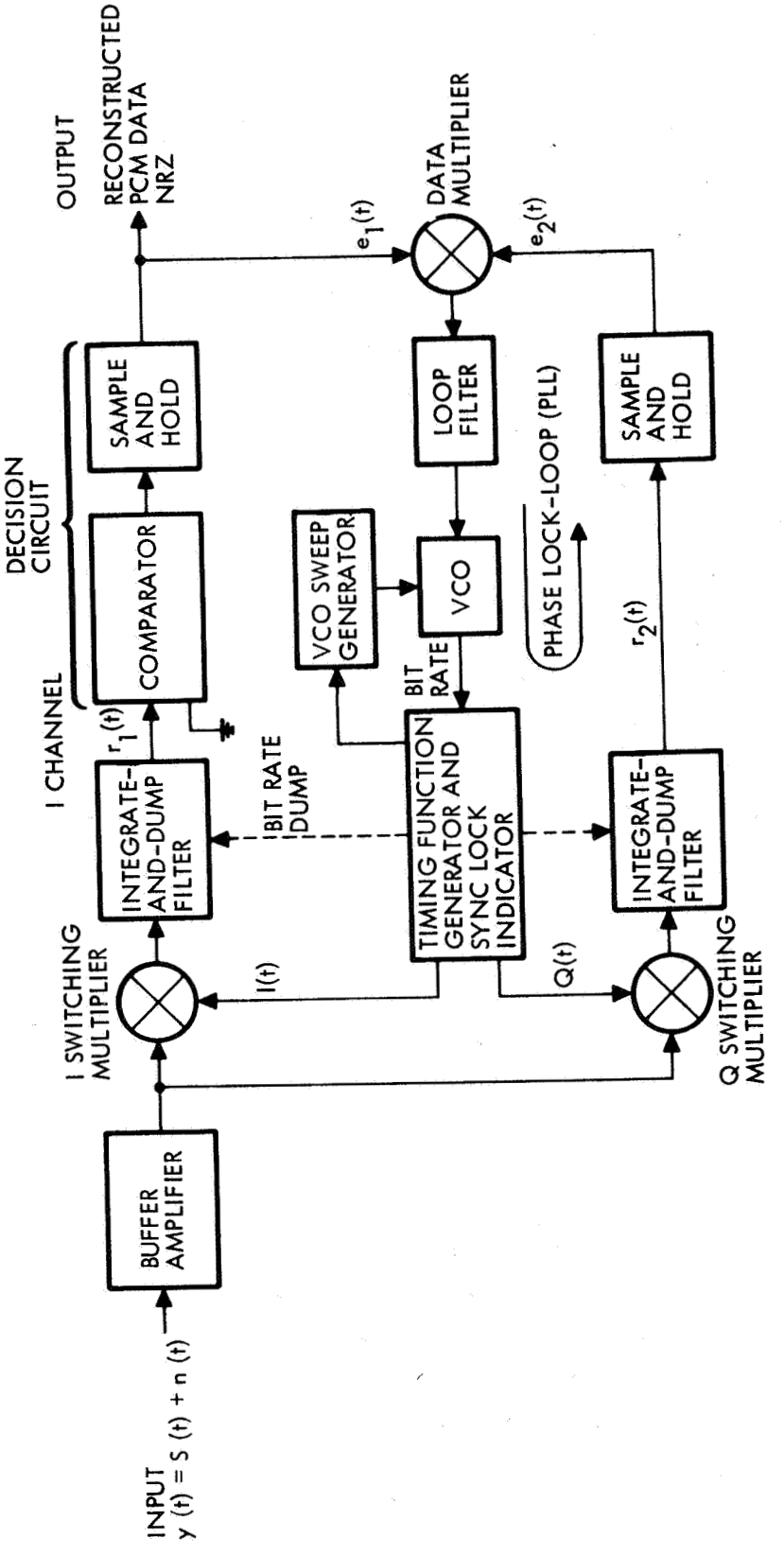


Figure D-4. I-Q Bit Synchronizer Block Diagram

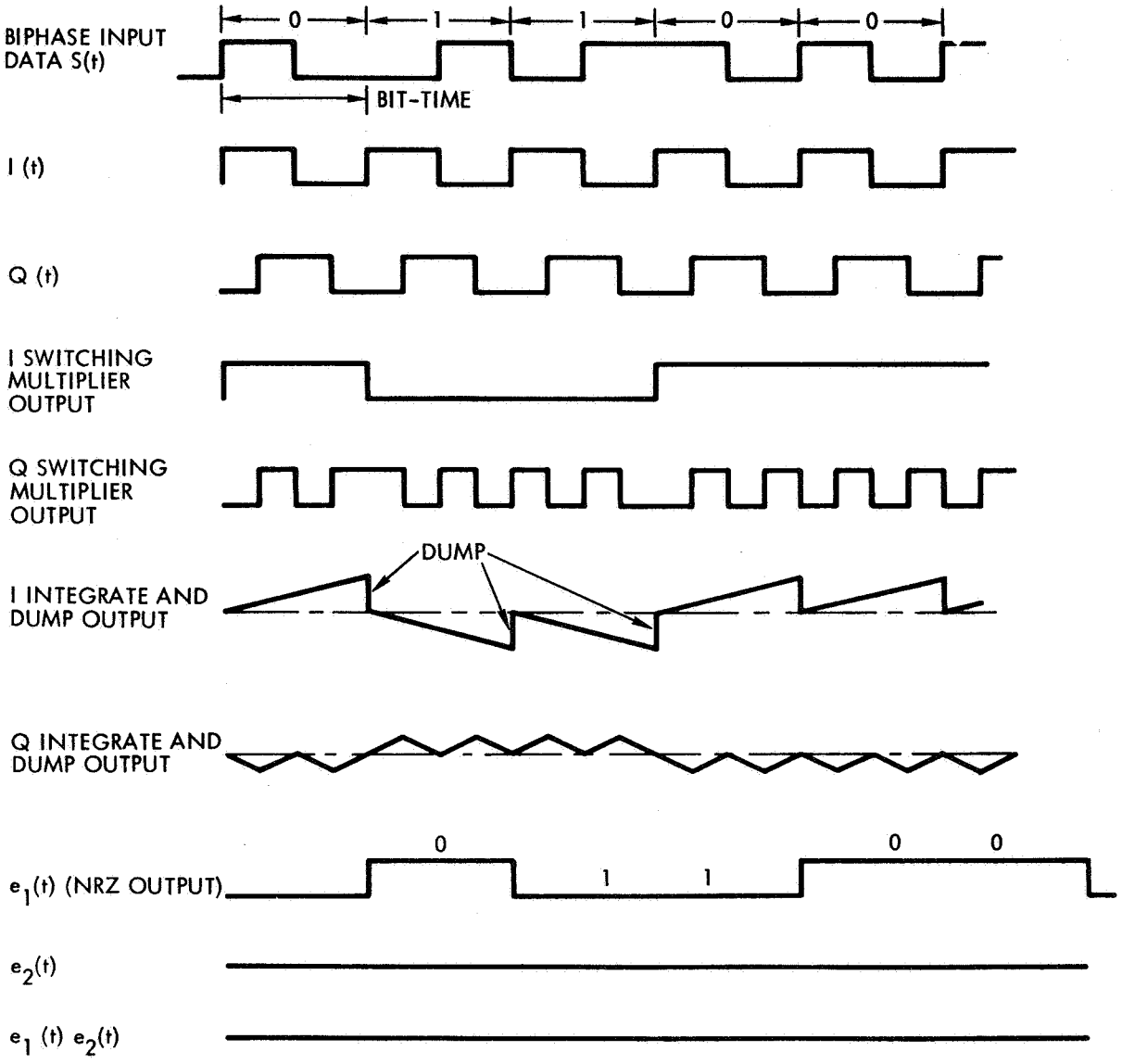


Figure D-5. Signal Waveforms for the I-Q Bit Synchronizer of the Phase-Lock Conditioner

The function of the Q channel is directly associated with the lock acquisition of the phase lock loop. In the lock condition the DC component of the Q channel output $e_2(t)$ is zero (as shown in Figure D-5). However, when the VCO waveform is out of phase by an amount ϕ, then it is easily verified that product $e_1(t)$, $e_2(t)$ will have a nonzero DC component. This condition is shown by the waveform diagram of Figure D-6, in which it is seen that the voltage polarity of the product of the NRZ output $e_1(t)$ (from the I channel) and $e_2(t)$(from the Q channel) is independent of the NRZ data itself. Hence, the proper polarity correction is applied to the VCO which drives the phase-lock loop in such a direction that the phase error ϕ is reduced towards zero and phase lock is achieved. The equivalent phase detector characteristic for the loop may be obtained by plotting e_1 and e_2 versus ϕ, as shown in Figure D-7. The phase detector characteristic exhibits stable nodes of true phase lock as well as stable nodes of false phase lock. The false lock conditions may be overcome by either taking advantage of the fact that the input signal split-phase waveform to the bit synchronizer always makes a transition at the middle of the bit period, or by utilizing the lack of true frame sync in the PCM telemetry data. Note also that when the input data is split phase this bit synchronizer does not depend on the occurrence of binary transitions in the input data to acquire bit synchronization.

Hence, the above discussion verifies that the proposed I-Q bit synchronizer configuration does offer a convenient and efficient technique for bit rate clock generation (by means of a phase-lock loop) and optimum binary data detection (by means of a matched filter). Performance, in terms of bit error rate, can be expected to approach the theoretical limits imposed by the curves of Figure D-1.

In the acquisition process of the phase-lock loop, an automatic sweep of the VCO is utilized to force the loop into bit rate synchronism (Figure D-4). This is accomplished by means of a sync lock indicator which controls the enabling and disabling of the VCO sweep circuit. In this way, the loop noise bandwidth (controlled by the loop filter) can be reduced as desired to improve steady state performance, i.e., to reduce the bit rate jitter of the VCO reference due to noise. However, the penalities for operating at low loop noise bandwidth are the lowering of the maximum

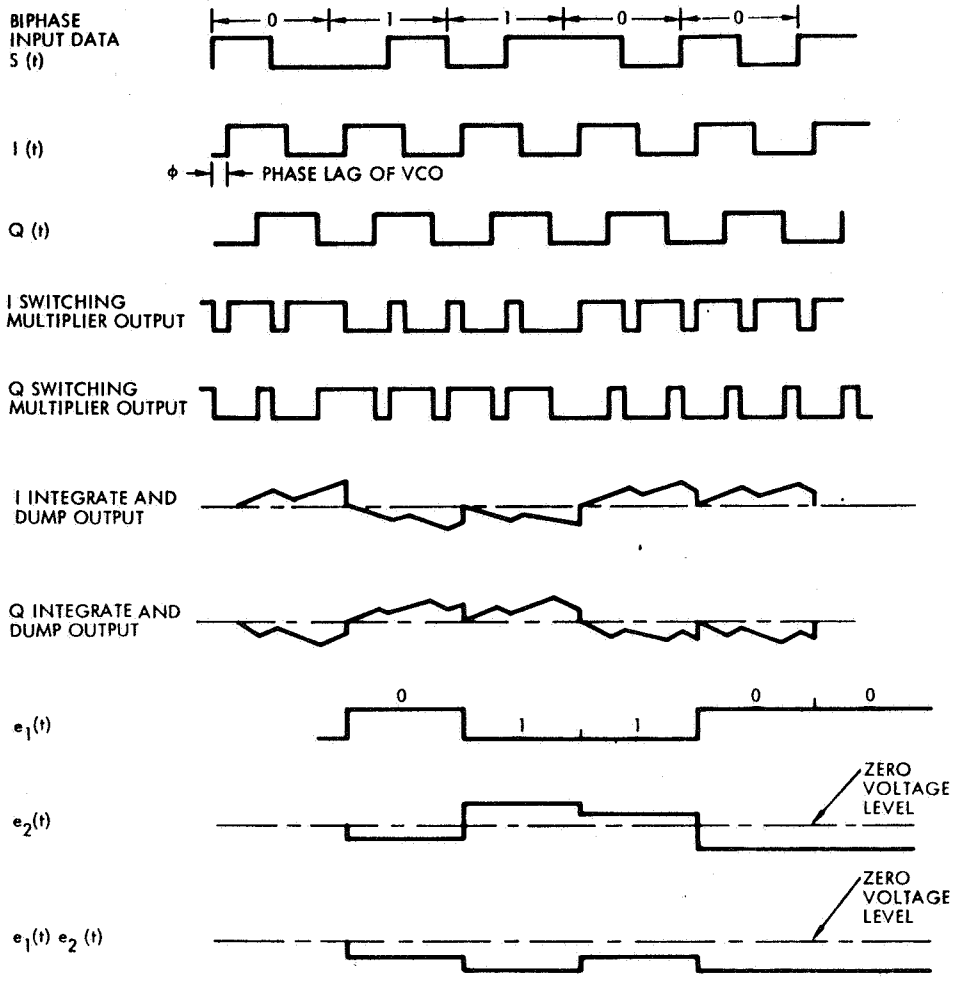


Figure D-6. Signal Waveforms for the I-Q Bit Synchronizer of Figure D-4; Lagging Reference Phase Condition

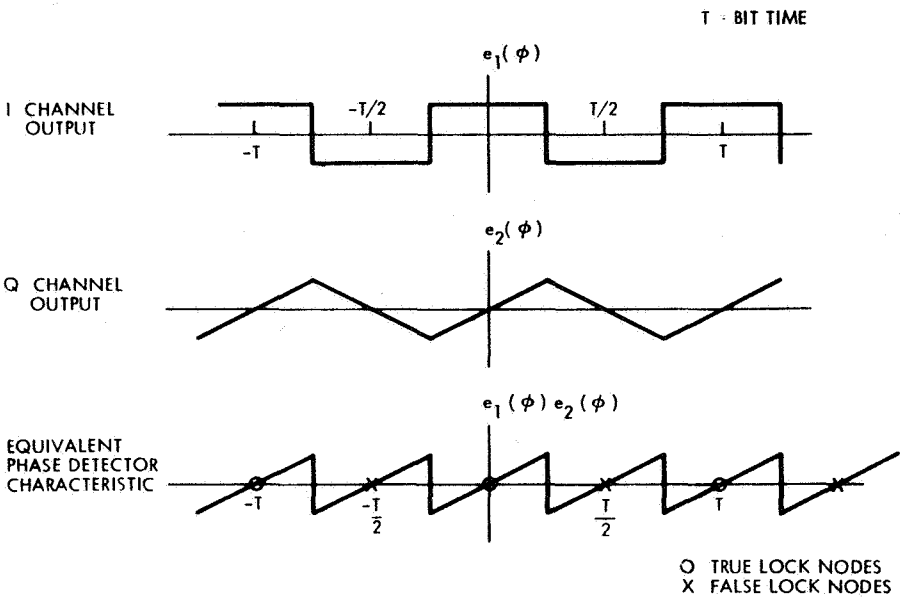
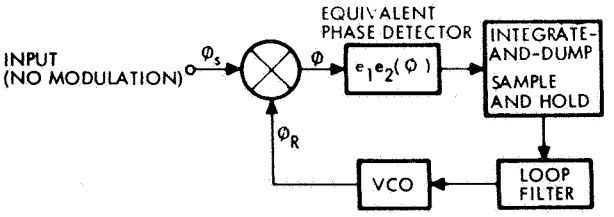


Figure D-7. Equivalent PLL Phase Detector Characteristic for the I-Q Bit Synchronizer System of Figure D-4

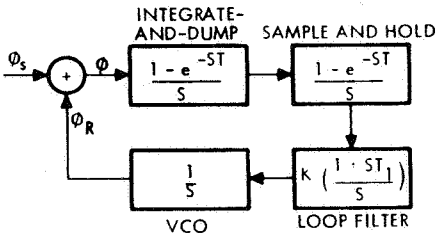
rate of change of input bit rate that can be tracked by the loop (without losing lock), and the rapid increase in acquisition time. This latter effect can be quite severe, since the average acquisition time when the VCO is swept in frequency is inversely proportional to w_n^2, where w_n is the loop bandwidth. It is possible to achieve a better tradeoff between loop bandwidth and acquisition time.

At large signal-to-noise ratio, Figure D-8 shows an equivalent model for the phase lock loop of the bit synchronizer in Figure D-4. Also shown is the small signal/equivalent linearized model for the in-lock condition. When the loop bandwidth is much smaller than the bit rate (as is usually the case to achieve good steady-state detection performance), the loop bandwidth and damping ratio are indicated in the figure.

The discussion of the I-Q bit synchronizer system has thus far been centered on the particular case where the input signal format is that of split-phase modulation. We consider next the case of NRZ input data. The block diagram of Figure D-4 may still be applied with the modification of reference timing waveforms I(t) and Q(t) to be I(t) = +1, and Q(t) = bit rate square wave, as shown in Figure D-9. Also shown is the equivalent



(A) EQUIVALENT FUNCTIONAL BLOCK DIAGRAM (LARGE SNR)



(B) MATHEMATICAL MODEL

LOOP BANDWIDTH $\omega_n = \sqrt{K}$

DAMPING RATIO $\xi = 1/2\,T_1\sqrt{K}$

K = EQUIVALENT LOOP GAIN

Figure D-8. Equivalent Mathematical Model for the Bit Synchronizer of Figure D-4

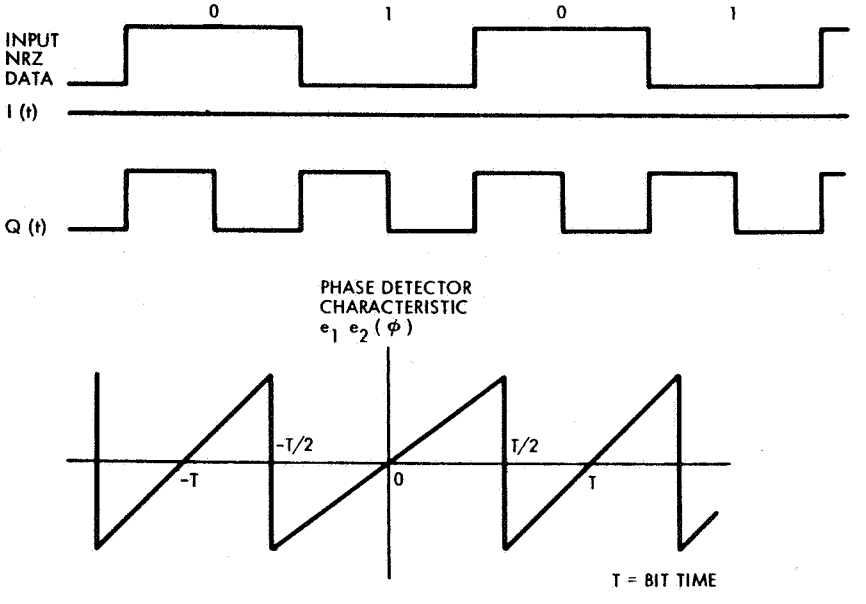


Figure D-9. Modifications to the I-Q Bit Synchronizer for the Case of NRZ Input Data

loop phase detector characteristic in the presence of data transitions every bit period. In contrast to the previous case of split-phase coding, the phase detector characteristic does not exhibit any conditions of false lock. However, loop acquisition does depend upon the transition density of the NRZ data. This dependency on information transitions is due to the following mechanism in the loop: when there are no transitions the signal input to the Q switching multiplier (Figure D-4) is constant so that $e_2 = 0$, and no corrections for loop phase error ϕ can be applied to the VCO. The effect of data transition density on loop acquisition can be approximately analyzed by deriving its average effect on the equivalent phase detector characteristic. The result, when the loop bandwidth is small compared to the bit rate, is that the equivalent phase detector gain is proportional to transition density M. Hence, the loop bandwidth and damping ratio (Figure D-8) in response to NRZ input data are each proportional to $M^{1/2}$. However, this argument cannot be applied to the loop response to noise (since in the absence of data transitions the input noise continues to excite the loop), and the loop equivalent noise bandwidth is proportional to $M^{-3/2}$. Thus, for the NRZ case, as one may expect, the presence of low transition density has the tendency to enhance the loop noise power with respect to the signal power, so that the VCO reference phase jitter increases and/or the lock acquisition time increases. It is possible to realize a better tradeoff by attempting to inhibit the noise excitation of the phase lock loop in the absence of data transitions. Thus, referring to Figure D-4, the data multiplier output (i.e., the loop correction voltage) can be forced to zero when a transition does not occur, or alternatively the sample and hold circuits can be maintained at their values corresponding to the last best estimate of loop correction in the presence of a transition. The relative merits of this technique for optimizing system performance in the presence of low transition density of NRZ data will be finalized during the development program.

Another attractive approach which avoids the problem of low transition densities (and its deleterious effect on the loop acquisition properties) is to utilize in the communication system the technique of subcarrier modulation of the NRZ data.

The operation of the proposed I-Q bit synchronizer to process RZ input data is closely related to its operation for NRZ data. As has been

discussed in Section 1, the theoretical detection performance for RZ data is 3 db poorer than for NRZ (since the RZ waveforms form an orthogonal code, or, equivalently, since the last half of the RZ bit waveform represents "no information"). Proper operation for the RZ format is obtained in the bit synchronizer by inhibiting the integrate and dump filters during the last half of the bit period, and instead having the sample and hold circuits continue holding during this time interval. The appropriate waveforms are shown in Figure D-10, and may be compared to waveforms for the NRZ case in Figure D-9.

2.3 PERFORMANCE ANALYSIS

To convey some preliminary technical information concerning the quantitative determination of acquisition and data detection performance of the proposed bit synchronizer system with respect to the theoretical or ideal performance, a brief description of the results to be expected is outlined below.

2.3.1 Detection DC Offset Errors

Consider first the detection degradation in the I-channel (Figure D-4) caused by undesired DC offsets of the buffer amplifier, switching multiplier, integrate and dump filter and comparator circuits. Let ΔE_{DC} be the total worst case DC offset voltage refered to the comparator (decision circuit) input at the end of the bit time and let A be the true signal voltage (for a "1") at this same point. Then, the bit error rate (BER) or bit error probability is easily shown to be given by

$$P_E = 1/2 \left\{ \phi[\lambda(1 + \delta)] + \phi[\lambda(1 - \delta)] \right\} \qquad \text{(D-13)}$$

where $\delta = \Delta E_{DC}/A$, λ^2 is the SNR defined by (I-4), and $\phi(\ )$ is the error function defined by Equation (D-3). The degradation in detection performance due to a nonzero DC offset ratio δ may be defined as the additional signal-to-noise ratio required to yield some specified error rate P_E. For example, if $\delta = 0.05$ then the degradation is 0.18 db, at an error rate of 10^{-4}. Parametric error rate curves versus signal-to-noise ratio for various offset ratios δ can easily be drawn (similar to Figure D-1) using Equation (D-13), from which the degradation in db is directly obtained. It

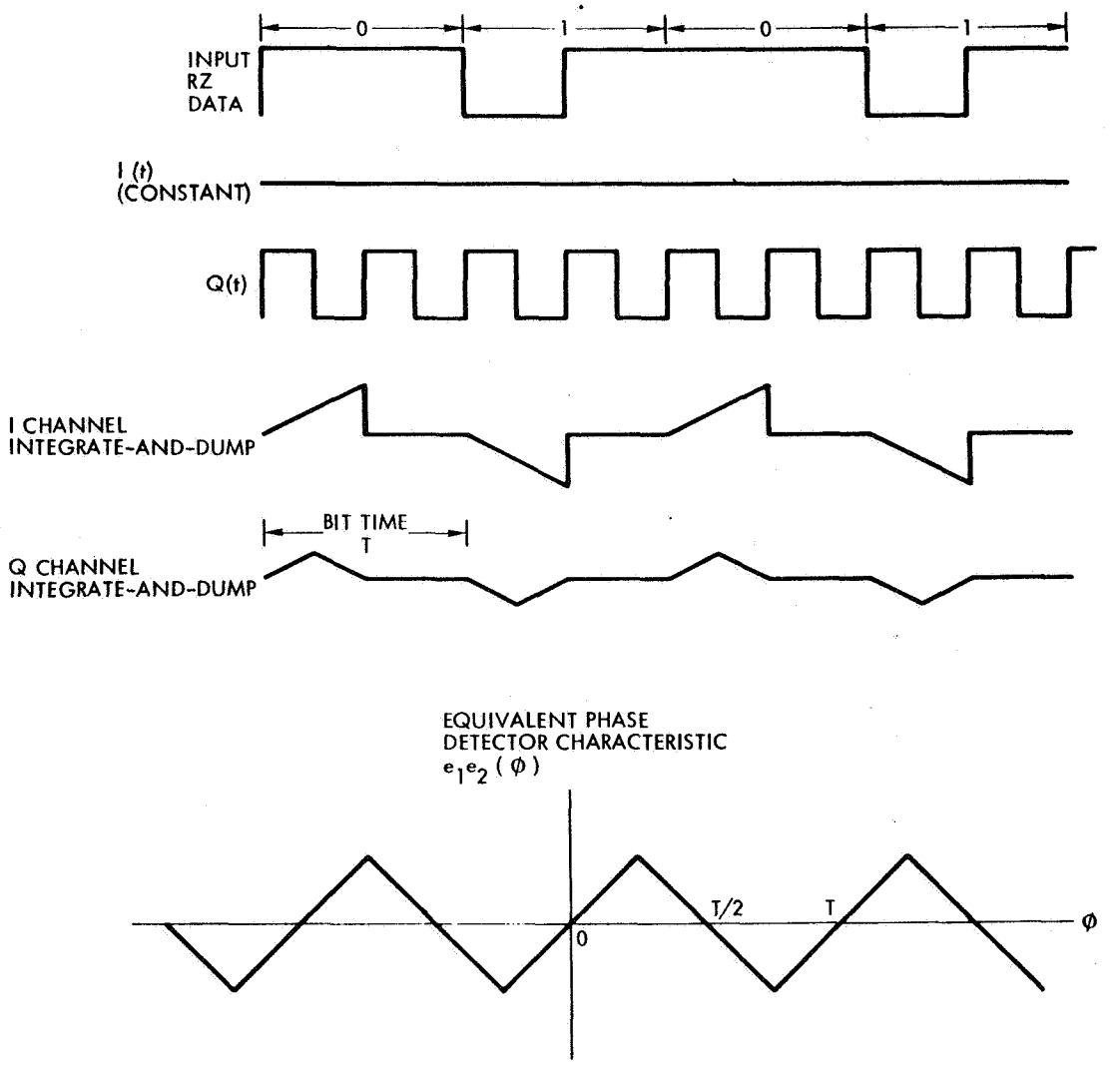


Figure D-10. Modifications to I-Q Bit Synchronizer for the Case of RZ Input Data

is estimated that in the worst case (over environmental and signal conditions) a maximum DC offset ratio of 0.04 is expected for the proposed bit synchronizer. This results in a degradation of 0.14 db.

2.3.2 Error Due to Switch Time Delays

There is a BER degradation associated with nonzero reset logic delays of the switching multiplier (if used) and integrate and dump circuits in the I-channel (Figure D-4). If t_d is the total delay of these switches,

then it is easily shown that the fractional degradation in signal-to-noise ratio at the integrate-and-dump output is equal to the ratio t_d/T, where T is the bit-time. For example, if the logic delays are 0.1 μsec, then the degradation is 0.01 db at a bit rate of 10^4 and 0.1 db at a bit rate of 10^5. The maximum degradation due to switch delays is approximately proportional to bit rate, with a loss of 0.25 db at 250 kHz and 1 db at 1.0 megabits/second.

2.3.3 Bit Rate Jitter

Consider first the effect of bit rate phase jitter in the bit synchronizer loop due to input additive white Gaussian noise (and not due to the presence of bit rate jitter on the input signal itself). The phase jitter of the dump timing signal to the integrate-and-dump circuit is obtained from the linearized system model of Figure D-8b. The resulting BER expression was indicated in Equation (D-7) for a 50 percent transition density of NRZ data. If the transition density is M, then this becomes

$$P_E = (1 - M)\,\phi(-\lambda) + 2M \int_0^\infty \phi\left(-\lambda + \frac{1}{\pi}\sqrt{\frac{B_O}{B_R}}\,y\right) \frac{e^{-1/2y^2}}{\sqrt{2\pi}}\,dy \quad \text{(D-14)}$$

For example, if M = 20 percent, and the ratio of loop noise bandwidth to bit rate is $B_O/B_R = 0.04$, then to achieve a BER of $P_E = 10^{-4}$, the signal-to-noise ratio must be $\lambda^2 = 8.35$ db. This is 0.1 db worse than the ideal case of no loop phase jitter (i.e., zero loop bandwidth).

The normalized time jitter (relative to the bit time T) of the dump time signal to the integrate-and-dump is given by

$$\sigma = \text{RMS relative time jitter} = \frac{1}{2\pi\lambda}\sqrt{\frac{B_O}{B_R}} \quad \text{(D-15)}$$

As discussed in Section 2, the theoretical BER for the bit synchronizer must take into account loop jitter due to input additive noise; therefore this theoretical BER is given by Equation (D-14). The actual performance degradation of the bit synchronizer is the equivalent amount of additional signal-to-noise ratio to achieve a prescribed measured BER as compared to the signal-to-noise ratio calculated from Equation (D-14).

Once a final selection of relative loop bandwidth B_O/B_R is made during the development program, the theoretical BER shall be then specified by Equation (D-14). The measured BER on the breadboard bit synchronizer model can then be compared with the theoretical BER at various transition densities.

2.3.4 Input Bit Rate Jitter

The analysis of loop response and degradation due to bit rate jitter present on the input signal itself to the bit synchronizer is very similar to the above analysis for loop jitter due to additive noise on the input signal. However, in order for the analysis to be completed, the exact nature of the input bit rate jitter must be specified. In particular, the power spectrum of the input jitter as well as its RMS value should be specified, since this has a direct bearing on the resulting performance degradation of the bit synchronizer in response to input jitter. For example, if the input jitter is actually a 25 percent peak-to-peak sinusoidal modulation of the bit period duration then at a data transition density of 50 percent, the degradation in detection performance is approximately 1.0 db. This assumes that the sine wave modulation is at a frequency greater than the loop bandwidth; for sine wave modulation at frequencies less than the loop bandwidth, the degradation shall be less since the loop tends to track out the bit rate variation. Using the model of Figure D-8, the loop phase error can be calculated in response to FM modulation of the input signal at a given modulation frequency and frequency deviation (i.e., jitter amplitude). This defines the calculated BER degradation due to the applied input bit rate jitter. A corresponding calculation will be made to determine the maximum amplitude and rate of sinusoidal (FM) input jitter for which lock is maintained at a given signal-to-noise ratio.

On the other hand, if the input bit rate jitter is due to a random effect and has a spectral bandwidth much greater than the loop bandwidth, the degradation for ±25 percent RMS input jitter is approximately 4.0 db. However, for smaller spectral bandwidths the degradation is less.

2.3.5 Acquisition and Tracking

The lock acquisition properties of the bit synchronizer include frequency capture range and average acquisition time (as a function of

signal-to-noise ratio and transition density). The tracking properties include tracking range maximum tracking rate and mean time to loss of lock (all as a function of signal-to-noise ratio). These properties are all intimately associated with the dynamics of the loop, in particular, of the loop bandwidth. The frequency capture and tracking ranges of the bit synchronizer will be 10 and 20 percent, respectively, in compliance with NASA/MSC specifications. The maximum tracking rate of a second order loop in the absence of noise is w_n^2 rad/sec^2 where w_n is the loop bandwidth; in the presence of noise, this maximum tracking rate is reduced by a factor which depends on the signal-to-noise ratio.

The above dynamic loop characteristics of the bit synchronizer will be finalized at the beginning of the program, once the necessary system tradeoffs are completed concerning the choice of the loop bandwidth/bit rate ratio and the acquisition technique.

Additionally, the maximum allowable rates for dynamic amplitude and baseline variations of the input signal to the bit synchronizer depends on the loop parameters chosen as well as the dynamic characteristics of the buffer amplifier (Figure D-4); these rates will be specified after the completion of the system design and tradeoff task.

3. DETAILED SYSTEM DESCRIPTION

3.1 GENERAL

Figure D-11 is a block diagram of the basic I-Q bit synchronizer. Here, integrate and dump (I and D) filters are assumed for ease of description of operation. Operation is essentially the same if additional blocks are cascaded with the I and D filters to optimize for nonsquare wave inputs.

The input PCM bit stream in the presence of noise is passed through a combination AGC amplifier and DC restorer to remove baseline offset and correct for variations in the signal amplitude. The output of the amplifier drives two 4-quadrant switching multipliers. The switch inputs to the multipliers are two functions, g1 and g2, which are derived logically, in time synchronism with the VCO. The waveforms of g1 and g2 depend on the input PCM codes to the bit synchronizer.

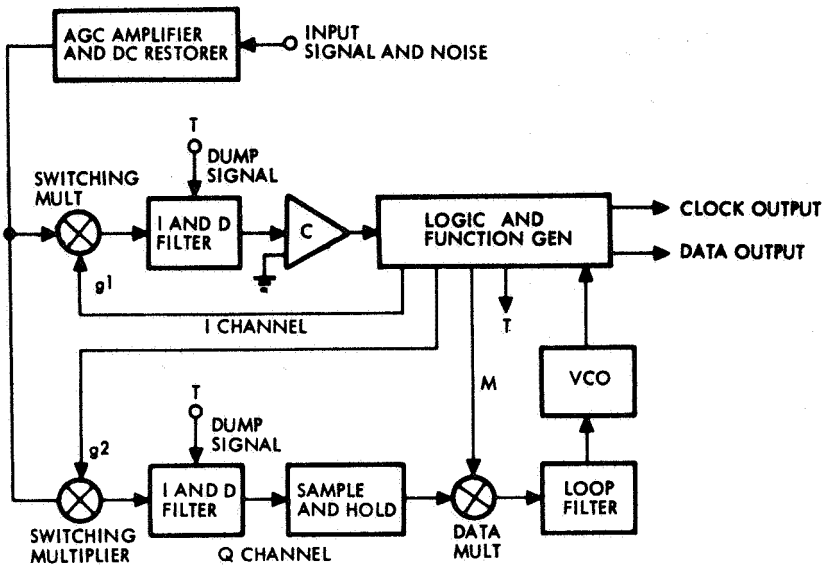


Figure D-11. I-Q Block Diagram Bit Synchronizer

The circuits following the upper switching multiplier of Figure D-1 (the I and D filter and the comparator) and the multiplier itself may be thought of as the "I" or in-phase channel. The province of the "I" channel is to maximize the S/N ratio at the output of the filter over the input bit time T. If we assume the integrator is reset at the bit times and the waveform of g1 is identical in frequency to the input waveform over a bit time, and is kept in phase synchronism with the input, then the S/N ratio will be maximized at the integrator output at the bit times. Sampling the I and D just prior to dump gives the best estimate of the information over the bit time.

Figure D-12 shows waveforms in the "I" channel for different input codes. For split phase (Manchester code), g1 is a square wave at the bit rate. For NRZ-M, g1 is a constant (since the input signal is a DC level over the bit time) so for this code or any similar code the "I" switching multiplier can be bypassed or removed from the circuit. Finally, for a code which is modulating a subcarrier of several cycles per bit, g1 is a square wave at the subcarrier rate. These waveforms are given to show

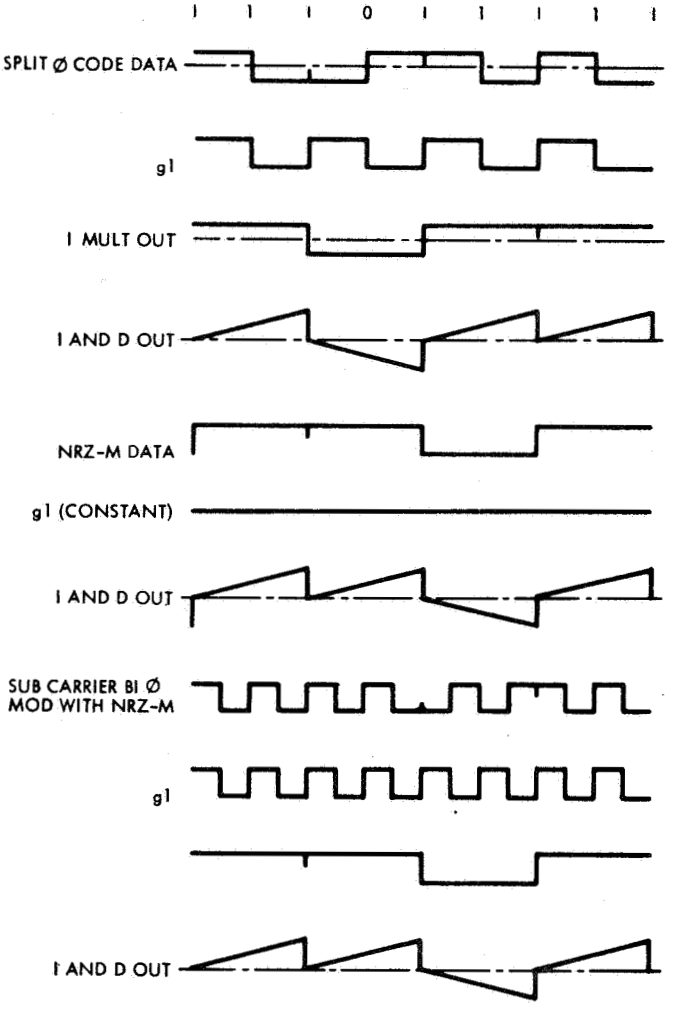


Figure D-12. Waveforms of I Channel with Various Input Codes

the ease with which a large class of code formats can be implemented by simple logical change of function generators. It will be seen later that the selection of g2, the synchronizing function, is equally simple.

The remainder of the circuit of Figure D-11 is the "Q" or quadrature channel which drives the VCO. If the proper function g2 is selected (depending on the input code), the output of the "Q" channel will supply sense information to the VCO driving it in phase/frequency synchronism with the input PCM. The polarity of the sense information to the VCO will depend on the PCM pattern at the input. The sense polarity will

reverse due to the bit transitions at the input, but similar reversals will occur in the "I" channel since it senses the same data. A third function "M" is generated in synchronism with the "I" channel data reversals and applied to a circuit called the data multiplier. This function and multiplier remove the unwanted reversals in the sense polarity, making it independent of data transitions. These concepts are further explained in the next section for an NRZ bit synchronizer.

3.2 SYNCHRONIZING TO NRZ

One requirement is for synchronization of NRZ data. This section describes an implementation of the synchronizer for this PCM code.

Figure D-13 is a block diagram of the NRZ bit synchronizer. The "I" channel consists of an I and D filter, followed by a high resolution comparator and a flip-flop. Since the NRZ code is a DC level over the bit time, g1 is a constant so that an "I" channel multiplier is not required.

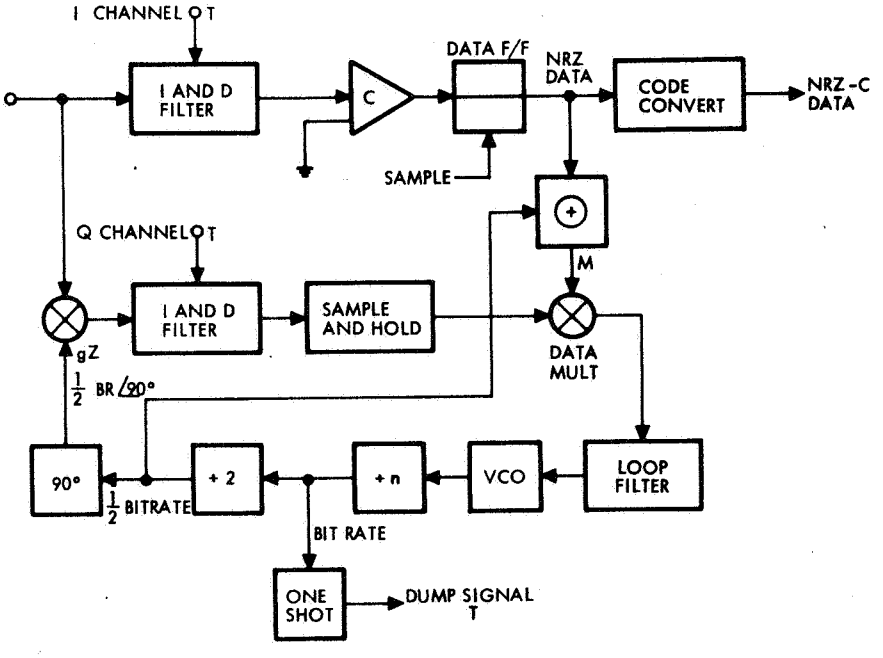


Figure D-13. NRZ Bit Synchronizer

The integrating filter is reset at the bit rate by a dump signal T derived from the locally generated reference (VCO). The "Q" channel multiplier is driven by a function g2 which is 1/2 the bit rate in frequency and shifted 90-degrees in phase (the transitions in g2 are centered between the dump signals). The data multiplier is driven by M which is the exclusive OR of the reconstructed NRZ data from the "I" channel and a locally generated signal at 1/2 the bit rate. This 1/2 bit rate signal is in phase with the dump signal. When function g2 is exactly 90 degrees out of phase with incoming bit information, the multiplier output is a square wave at twice the data frequency. The sampled and held output of the integrator is zero and, hence, no correction voltage is supplied to the VCO, thus indicating bit synchronism. Under these conditions the integrators are being reset exactly at the bit transitions and the data FF is being sampled just prior to dump, providing optimum detection. For phase errors at the input, the multiplier output contains DC components which are integrated, sampled, and held, and applied to the VCO after removal of polarity ambiguities by the data multiplier. The correction voltage applied to the VCO drives it back in to phase synchronism with the input. Figure D-14 shows the major waveforms of the NRZ bit synchronizer drawn for a phase error at the input. The waveforms are drawn for NRZ-M input data, but hold for NRZ-S or NRZ-C. The only difference is the output code converter. It is well understood that the NRZ-C code, being nondifferential, when phase-modulating a carrier, requires the receiver to supply the correct carrier phase or the bit synchronizer output will be inverted. This can be resolved by using the frame sync signal from the decommutation equipment to reverse the data polarity of the bit sync when loss of frame sync occurs.

3.3 SYNCHRONIZING TO SPLIT PHASE

The synchronizer discussed will handle the split phase code by making g1 a function of frequency equal to the bit rate and in phase with the dump signal and making g2 equal in frequency to g1 but shifted 90 degrees in phase with respect to it.

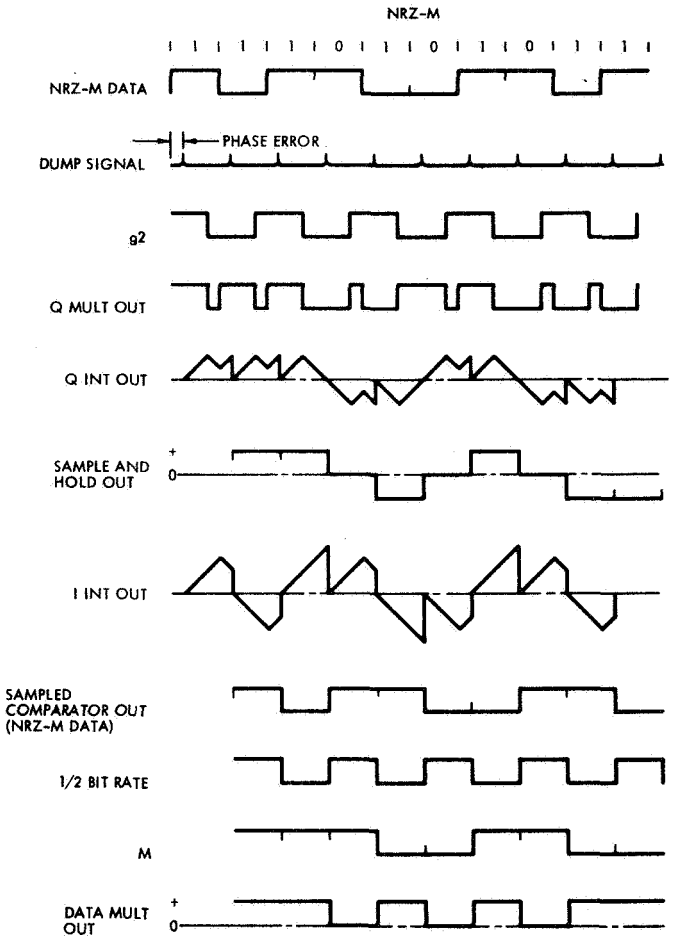


Figure D-14. Waveforms of NRZ Bit Synchronizer Drawn for Phase Shift Between Input and Locally Generated Reference

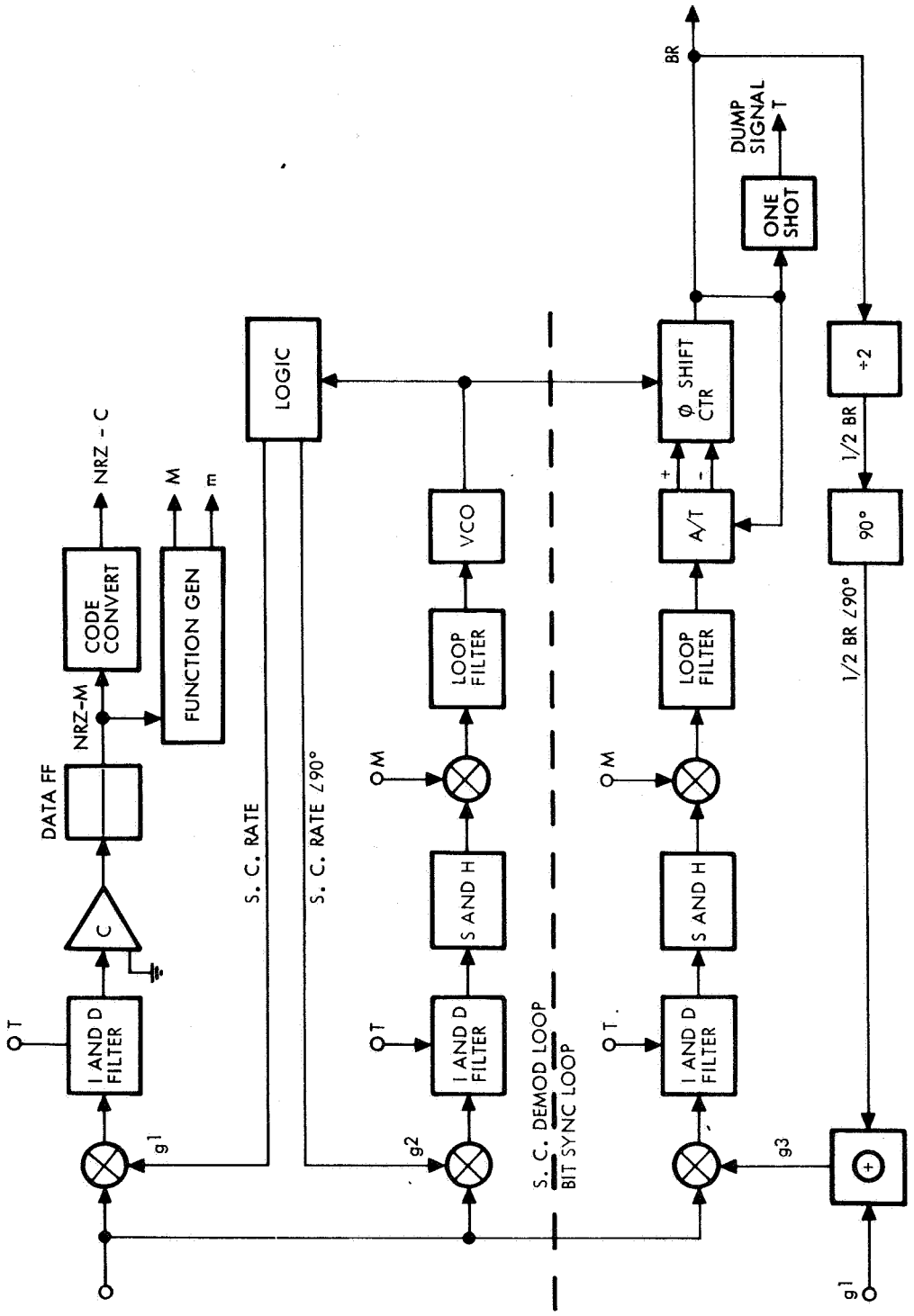


Figure D-15. Block Diagram Subcarrier Demodulator Bit Synchronizer

Like the NRZ-C code, split phase is nondifferential (it is basically a subcarrier with frequency equal to the bit rate, which is phase modulated by NRZ-C data), so the polarity of the output code depends on the absolute phase between the input and the reference functions. Again, the frame sync signal from the decommutation equipment can be used to automatically resolve this ambiguity since its occurrence is recognized by the presence of the complement of the frame sync code. Other methods of resolving the phase are available. One method is to count odd and even transitions and compare them. Because the mid bit transitions occur in every bit, and because the data transitions occur less often, a logical function is generated to force the output data to assume the polarity corresponding to the proper transition tally.

3.4 SYNCHRONIZING TO PCM DATA ON A PHASE MODULATED SUBCARRIER

The basic I-Q bit synchronizer can be used to synchronously demodulate PCM data phase modulated on a subcarrier of n cycles per bit. There are phase ambiguities equal to the number n of subcarrier cycles per bit which, if a differential PCM code is used, can be resolved by the addition of a second quadrature loop. If a nondifferential code is used, other information such as a frame sync signal is necessary in addition to the second Q loop. An example of the latter case is the split phase code (one subcarrier cycle per bit with NRZ-C modulation).

Figure D-15 is a block diagram of the I-Q bit synchronizer modified to demodulate subcarrier modulated NRZ data. The diagram is broken into two parts or loops; the upper loop is called the subcarrier demodulator loop and the lower loop is called the bit synchronizer loop. Operation of the subcarrier demodulator loop is as discussed previously for the NRZ bit synchronizer, except where g1 is a locally generated reference at the subcarrier frequency, and g2 is at the same frequency but phase shifted in quadrature with g1. When the integrators are being reset at the bit times (bit sync established), this loop will optimally detect the bit information even if the subcarrier of interest is frequency multiplexed with subcarriers at adjacent frequencies. If one wishes to transmit frequency multiplexed square wave subcarriers, the loop will optimally

detect them, the only requirement being that the dynamic range of the input circuits is large enough to handle the large noise levels from the receiver without excessive limiting.

It is easy to verify, referring to Figure D-15, that a single design, utilizing plug-in or switching modules, will cover a large range of subcarriers. The g functions are changed by logical switching, and circuit scale factors and loop parameters changed by switching discrete components in the analog circuits.

The bit synchronization loop operates like the demodulator loop, since it shares the demodulator I loop for the derivation of the data multiplier signal m, the difference being in the derivation of the multiplier signal g3. This signal is the Exclusive OR of g1 and a signal of 1/2 bit rate shifted 90 degrees for NRZ-M data.

The signal g3 can be thought of as the "digital product" of g1 and 1/2 bit rate ∠90 degrees where g1 demodulates the subcarrier producing NRZ data and 1/2 bit rate ∠90 degrees synchronizes to the NRZ. The same result would be achieved by cascading two switching multipliers and driving each with the components of g3. This is undesirable because, in addition to circuit complexity, the second multiplier (receiving the demodulated NRZ) would have to be DC coupled.

Several methods are available for implementing the bit sync loop. The method shown in Figure D-15 is to include a phase-shift counter driven from the VCO. If the input code consists of an integral number of cycles per bit, the bit rate is available when the demodulator is in lock and the bit sync has only to resolve the phase. If subcarrier and bit rate are noncoherent, a separate bit sync VCO is required.

In the bit synchronizer of Figure D-15 error voltages out of the loop filter are impressed on an analog-to-time gate converter. This circuit is a simple ramp encoder, which converts the error voltage to a gate pulse of width proportional to the error and supplies the pulse as an output on one of two lines, depending on whether the error was positive or negative. The pulses go to a phase-shift counter which counts down to the bit rate from the VCO rate. The input stages of the counter will divide by 2, 4, or stop for periods of time, depending on the width of the

gate pulse and which line it is on. For error of one polarity the output phase of the counter will be advanced. An error of the other polarity will retard it. When no error exists, the counter will hold its phase. If a separate VCO is used, it is driven directly from the filter.

The demodulator synchronizer designed by TRW for the Pioneer program uses a separate bit sync VCO. The TRW unit for another program uses a separate bit sync VCO. The TRW unit for another program uses the phase shifter technique described for Figure D-15.

3.5 SYSTEM DESIGN APPROACH

Figure D-16 is a detailed block diagram of the recommended PCM bit synchronizer. The unit shown is capable of operating, on command, at any 2 bit rates in binary multiples from 8 bits/sec to 1 Mb/sec. Intermediate bit rates are obtained by changing the VCO quiescent frequency. The PCM codes can be NRZ-M, NRZ-S, NRZ-C, split-phase, or RZ. It is also capable o demodulating, on command, one of two telemetry subcarriers which are biphase modulated by NRZ PCM data. The modulating bit rate range is 8 bits/sec to 8 kbits/sec. The subcarrier rates can be chosen in binary multiples of the bit rates. For example, 8 bits/sec data can be demodulated from subcarriers of 32 cycles/sec, 64 cycles/sec, 2048 cycles/sec, etc., depending on where in the frequency spectrum it is desired to place the subcarrier.

The flexibility is obtained by preflight patching of logical functions to obtain the variety of functions (g1, g2, g3, etc.) required to synchronize to the various code formats. Unused portions of the unit (logic modules or subassemblies) are eliminated in the assembly, minimizing the hardware required in flight.

Table D-1 is a format schedule which shows the required patching as a function of code format. Figures D-14, D-17, D-18, D-19, and D-20 show the major waveforms of the unit for the different input codes and selected functions of Table D-1. The I and D sample and hold wave forms are over-simplified for ease of description. They show dump periods which are very small compared to a bit period. This is impossible at the high bit rates and tight performance requirements specified here;

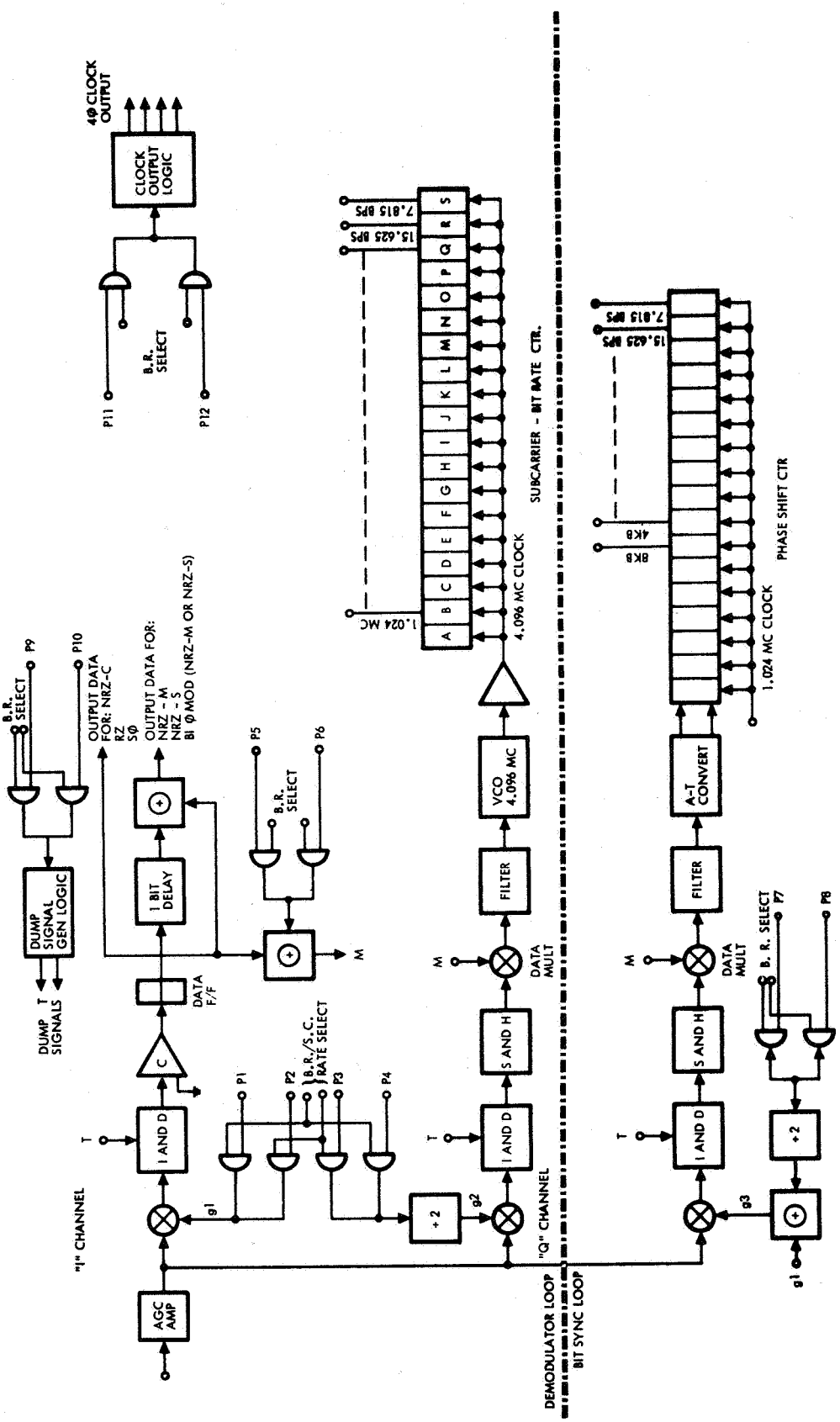


Figure D-16. Flexible PCM Bit Synchronizer

instead, time-shared filters will be used, with the appropriate timing being generated in dump signal generation logic. Dual integrators are used in the "I" channel, each one integrating and being dumped on alternate bit periods. Triple integrators are used in the "Q" channels, each one integrating, holding the integrated quantity, and being dumped, on each third bit period. This allows a minimum of 1 microsecond for each of the dump and hold functions.

Table D-1. Format Schedule

Function	Code Format			
	NRZ	BI ϕMOD Subcarrier	Split ϕ	RZ
g_1	Constant - Remove "I" mult and associated logic	Patch appropriate subcarrier freqs. to P1 and P2 from subcarrier counter remove unused parts of counter	Patch appropriate bit rate signals to P1 and P2 from bit rate counter. Remove unused parts of counter	Constant - Remove "I" mult and associated logic
g_2	Patch 1/2 bit rate signals from bit rate counter to P3 and P4	Patch subcarrier freqs. from subcarrier counter to P3 and P4	Patch bit rate signals from bit rate counter to P3 and P4	Patch bit rate signal from bit rate counter to P3 and P4
g_3	Eliminate bit sync loop subassembly	Patch bit rate signals from phase shift counter to P7 and P8	Same as for NRZ	Same as for NRZ
M	Patch bit rate signals from bit rate counter to P5 and P6	Patch bit rate signals from phase shift counter to P5 and P6	Remove logic associated with M and drive data mult with output of data F/F	Same as Split ϕ
T	Patch bit rate signals from bit rate counter to P9 and P10	Patch bit rate signals from subcarrier counter to P9 and P10	Same as NRZ	Patch 2 x bit rate signal from bit rate counter to P9 and P10
Clock Out	Patch 4 x bit rate signals from bit rate counter to P11 and P12	Patch 4 x bit rate signals from phase shifter to P11 and P12	Same as NRZ	Same as NRZ

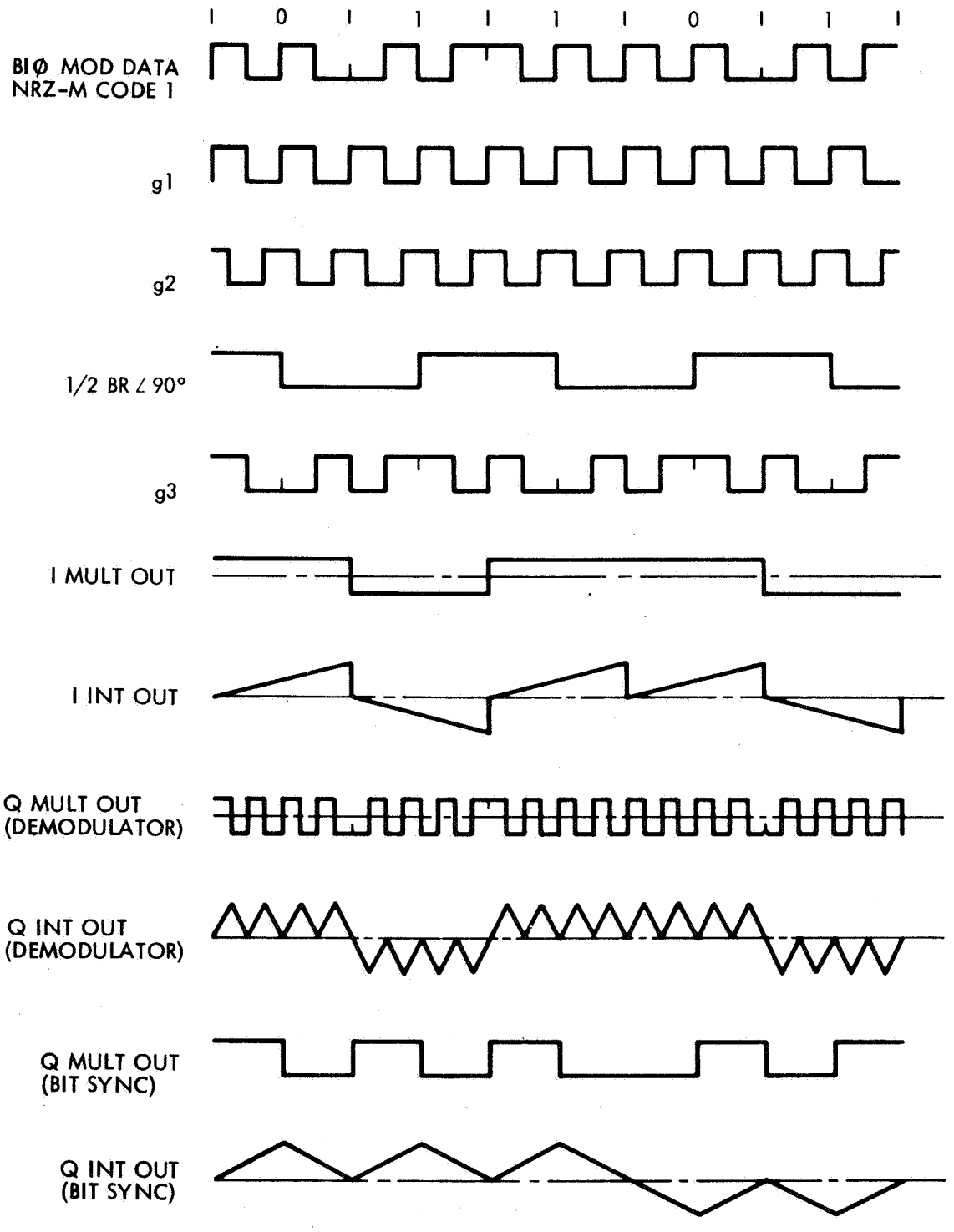


Figure D-17. Waveforms of Bi-Phase Demod Sync Drawn for in Synchronism Condition. Two Subcarrier Cycles Per Bit Period NRZ-M Data

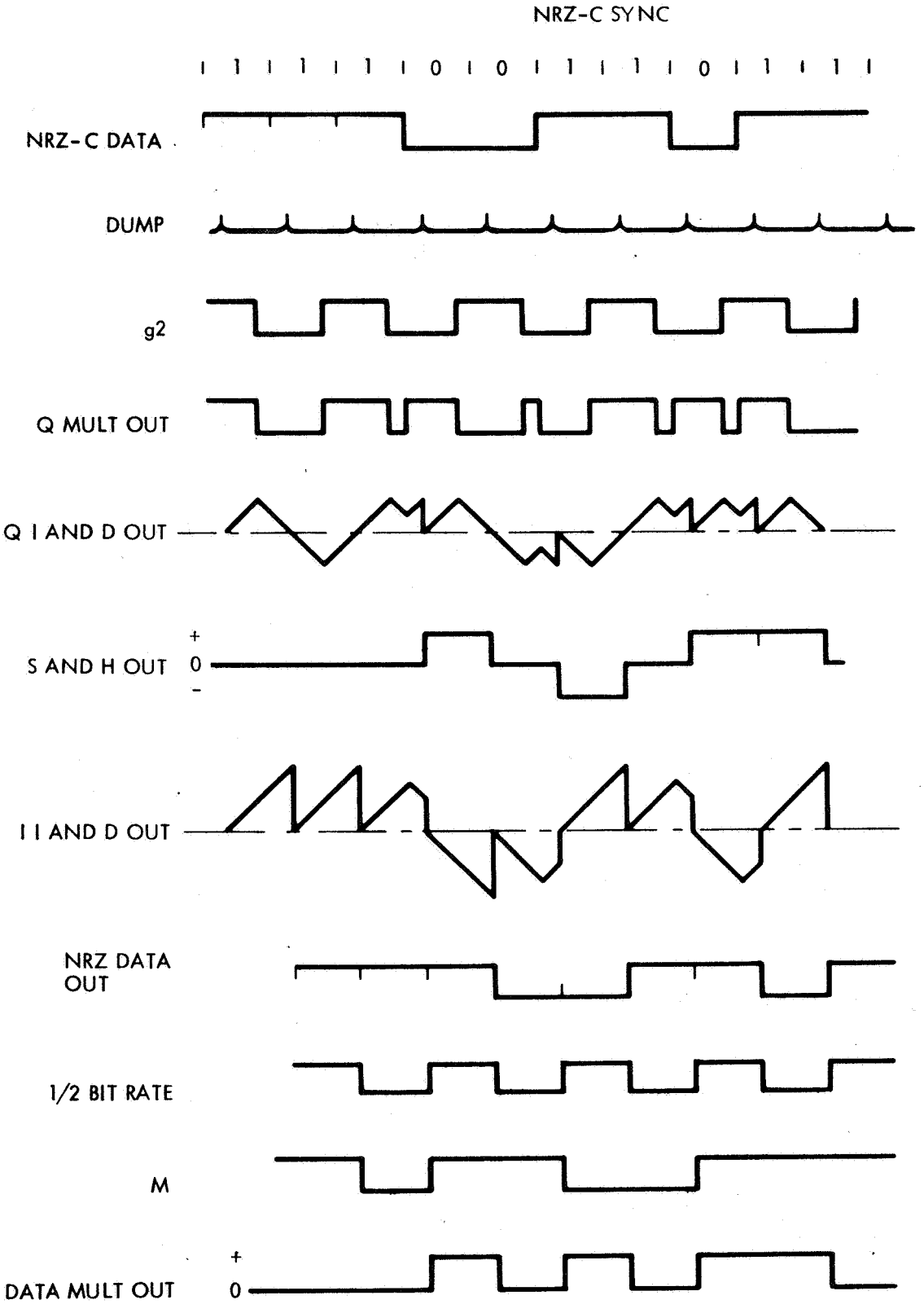


Figure D-18. Waveforms for NRZ-C Code

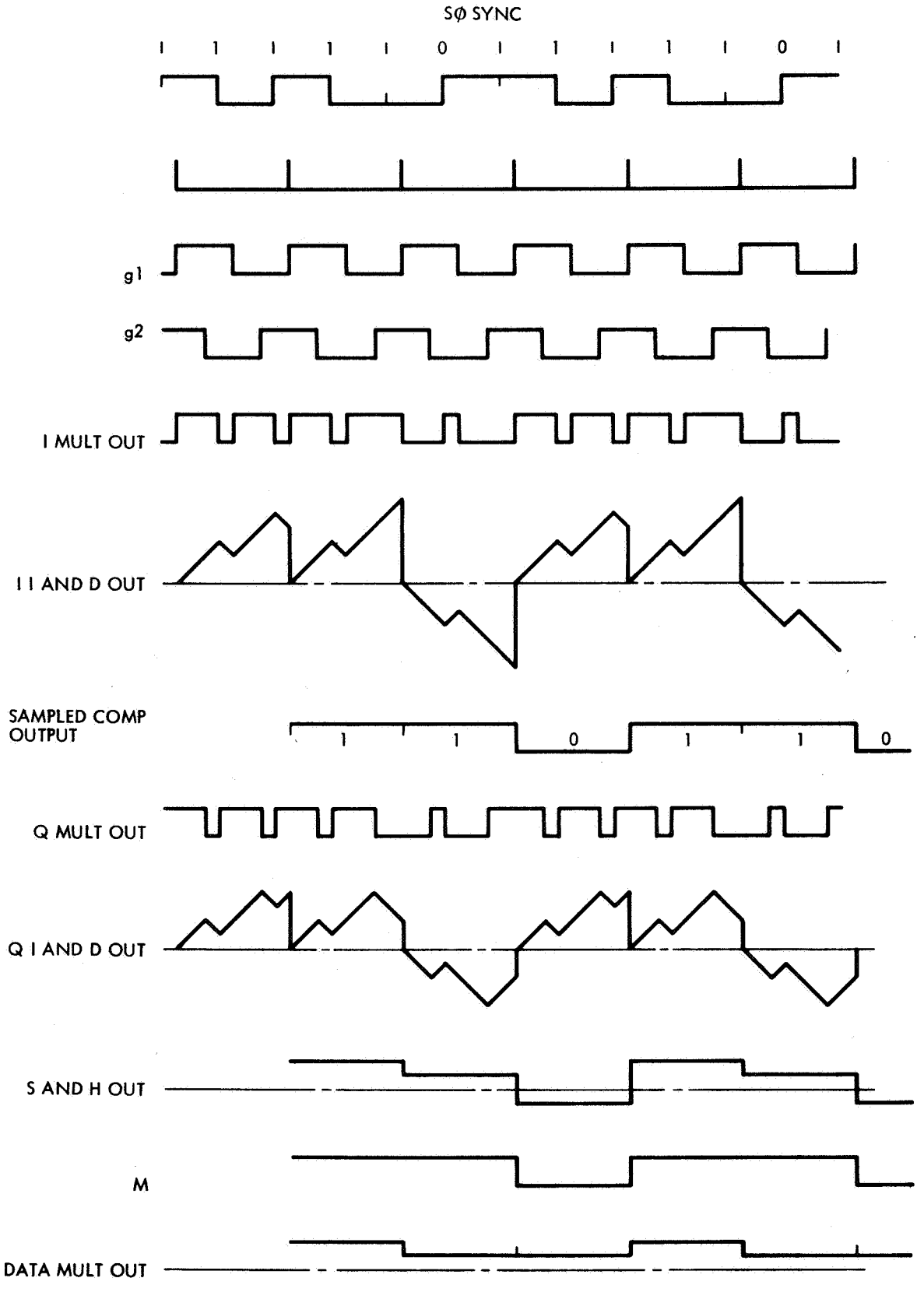


Figure D-19. Waveforms for Sϕ Code

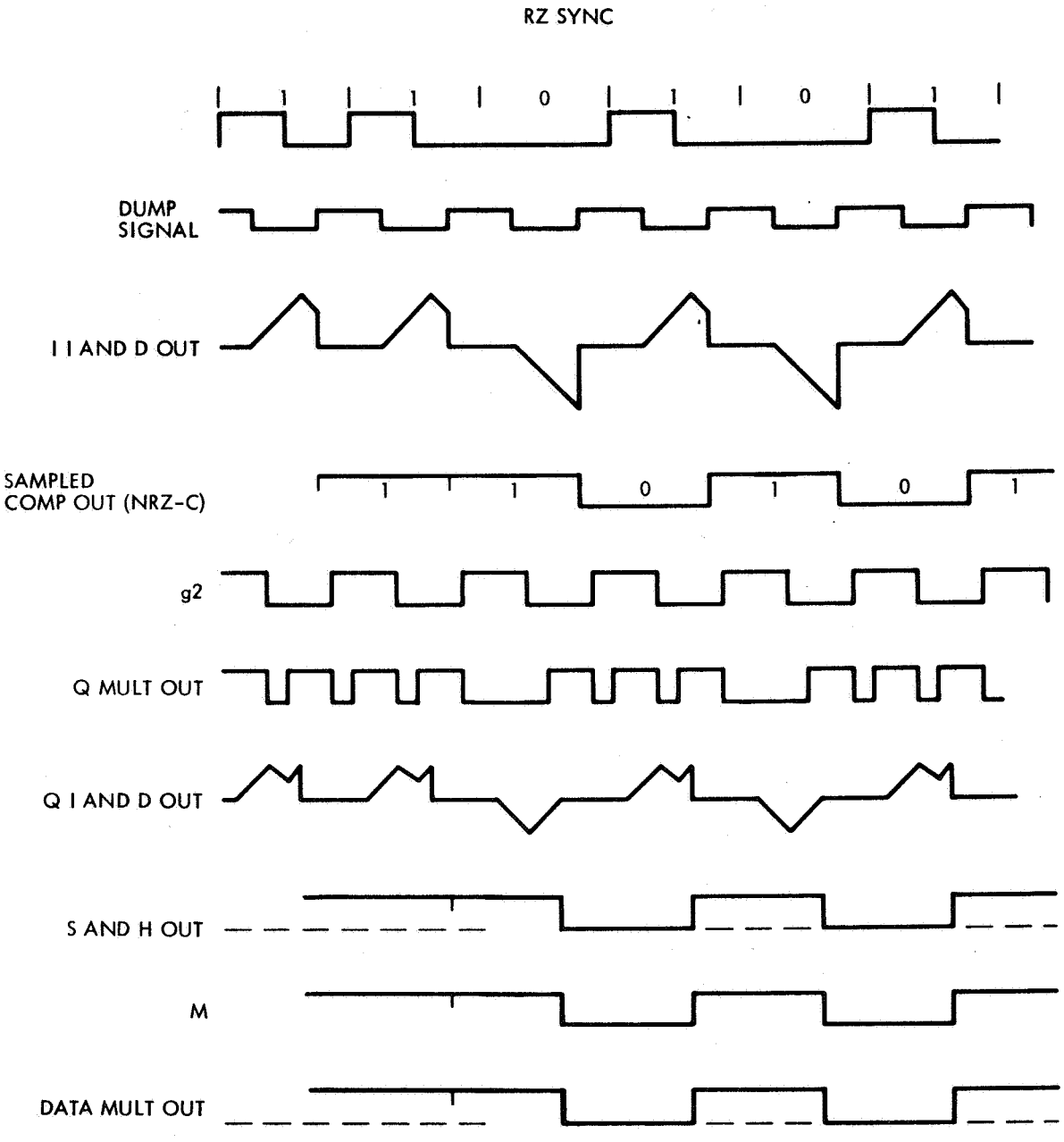


Figure D-20. Waveforms for RZ Code

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APPENDIX E

COAST PHASE ATTITUDE CONTROL ANALYSIS

This section describes the analytical studies and tradeoff investigations leading to the selection of the recommended guidance and control subsystem configuration and the various hardware components.

1. CONTROL MODES

For the Voyager control system, two fundamental analog circuits and their combinations were considered for supplying control system damping. These were a lead-lag switching circuit design and a derived rate increment (DRI) modulator design. The lead-lag circuit is optimum with large control errors, and the DRI is optimum in the small. Tradeoff studies were conducted to find the best means of combining them for operation throughout the whole range of Voyager control modes.

The lead-lag circuit is shown in Figure E-1. Essentially, the jets are "on" outside the deadzone and "off" within it. In this study, the parameters were chosen for rapid in-the-large convergence. The sensitivity of the lead-lag design to jet valve delays, vehicle dynamics uncertainties, and optical sensor anomalies makes it less desirable for use during the cruise mode.

The DRI design shown in Figure E-2 consists of a switching circuit with a feedback lag filter. The circuit parameters are selected to produce the desired minimum on-time pulsing of the attitude control jets for small attitude and rate errors. For larger errors, the pulses become longer in duration, eventually reaching a full-on state for extremely large errors. Use of the DRI circuit is particularly attractive during the cruise mode where rate damping is needed with minimum on-time pulsing in order to maintain low gas consumption. Vehicle rates during cruise may be less than 0.3 degree per hour, and rate information at these low levels is uncertain. The damping provided by the circuit is proportional to the lag filter time constant; hence, large values are desired when rate information is not available and it is the only

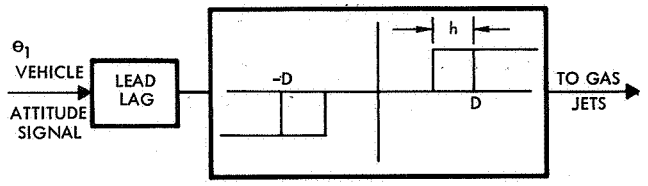


Figure E-1. Lead-Lag Switching Circuit Block Diagram Showing Deadband, D, and Hysteresis, H

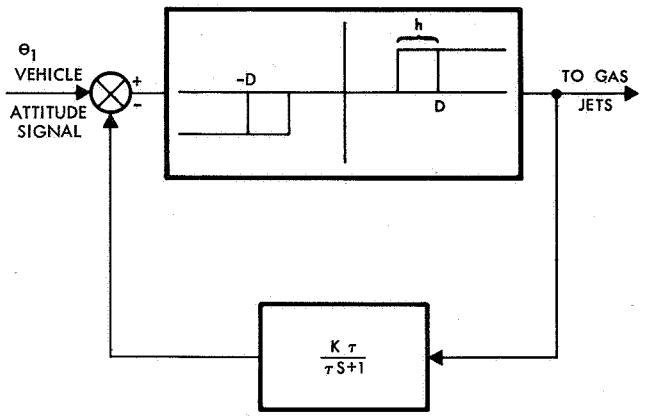


Figure E-2. Derived Rate Increment Modulator

source of system damping. Typical values range between 50 to 80 seconds in spacecraft designs. Values larger than this are difficult to implement and maintain for long operating durations. Values smaller than this increase the possibility of inadvertent multiple pulsing due to extraneous system noise and disturbances and reduce system damping such that poorer convergence from initial conditions results.

The designs investigated were selected such that, if a mode switch failed, backup rate compensation for system damping would be provided even though an associated performance degradation could ensue. With this design goal, the circuits considered were the switched DRI feedback, parallel DRI/lead-lag, switched DRI/lead-lag, and series DRI/lead-lag designs shown respectively in Figures E-3, E-4, E-5, and E-6. The phase plane switching lines for the inertial hold mode are also indicated in these figures.

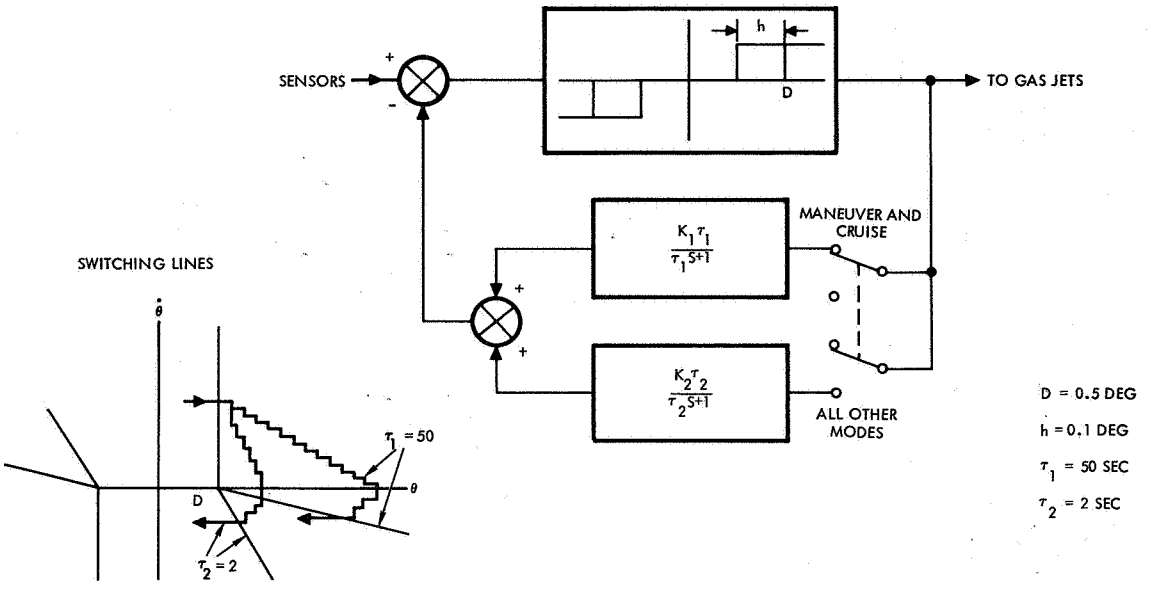


Figure E-3. DR1 Feedback Design Block Diagram and Phase Plane Switching Lines

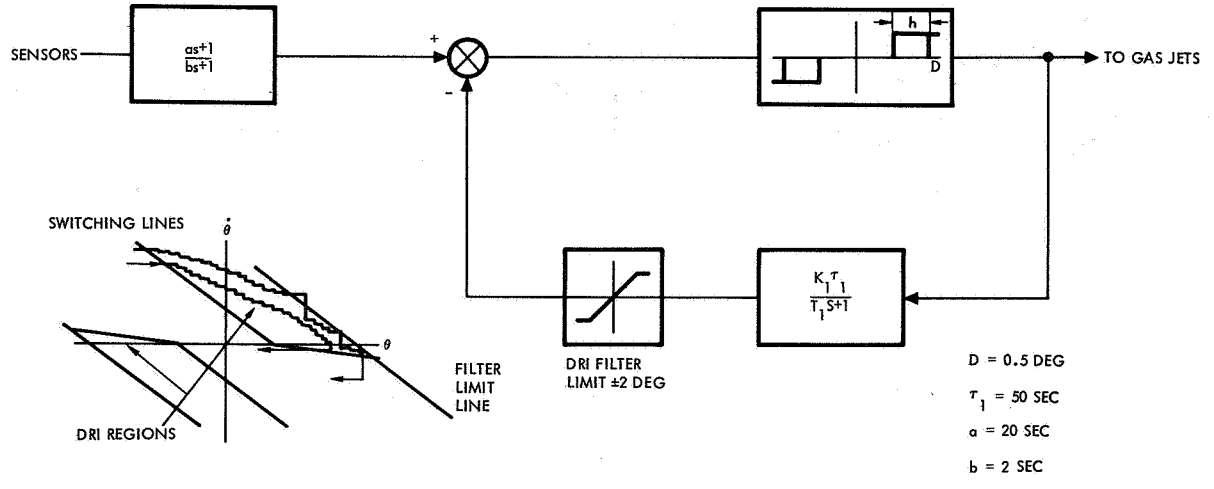


Figure E-4. Parallel DRI/Lead-Lag Design Block Diagram and Phase Plane Switching Lines

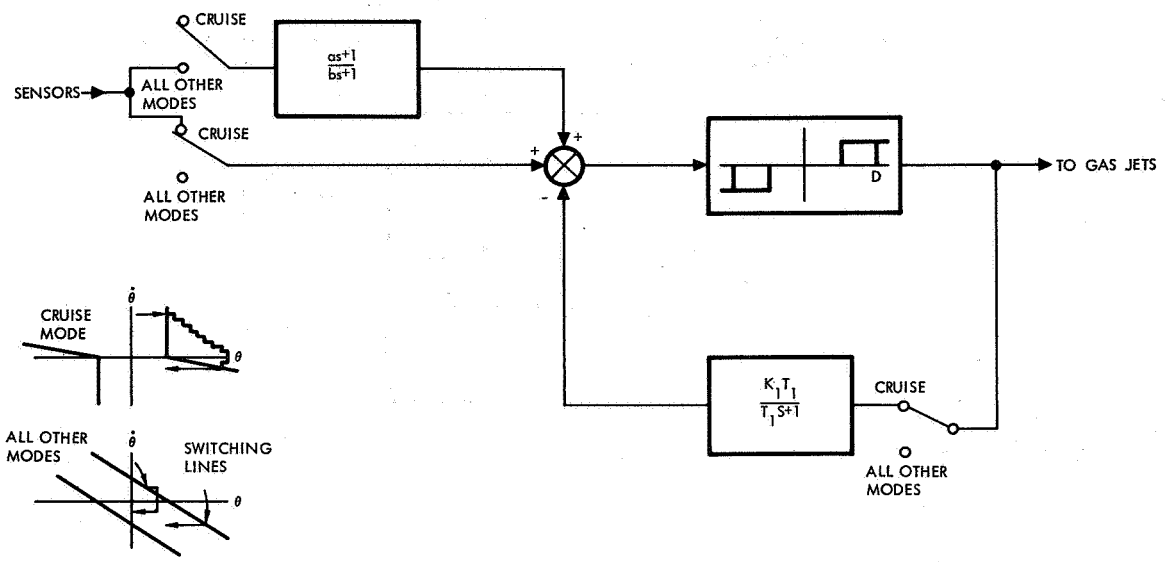


Figure E-5. Switched DRI/Lead-Lag Filter

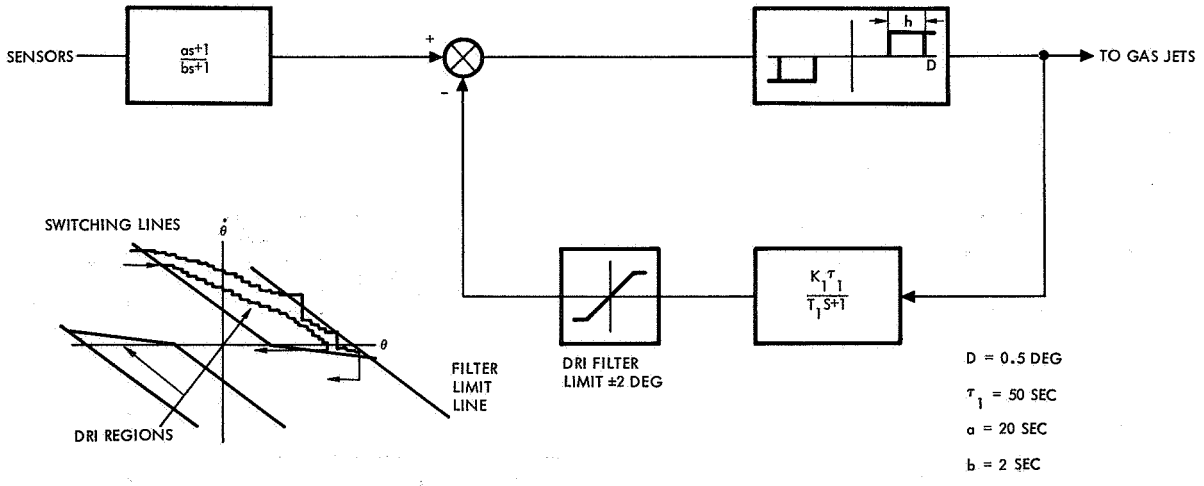


Figure E-6. Series DRI/Lead-Lag Filter

In the switched DRI feedback design, a two-second DRI time constant circuit is employed for all modes in which rate gyros are in use; otherwise, overdamped and sluggish responses occur during separation and acquisition operations. Rate damping is not required from the circuit except as a backup damping measure. The value of two seconds was arbitrarily selected for investigation. For the cruise mode and for reorientation maneuvers where position gyros are used and where circuit rate damping is required, a large time constant of 50 seconds is employed. The switched DRI design was not as desirable as the other designs since a single thruster failure during a maneuver could cause a large gyro error, sufficient to reach its limit. Also, the fuel and time consumed during maneuvers were considerably greater than with the other designs.

The switched DRI/lead-lag design is straightforward with the lead-lag circuit employed in all modes other than cruise. The desirability of the lead-lag filter, particularly during maneuvers, was clearly indicated in simulation studies. A switch to the DRI circuit is made for the cruise modes.

The series DRI/lead-lag design employs a DRI circuit for cruise mode operation with additional series lead-lag filtering to provide rate damping during maneuvers. A DRI time constant of 50 seconds is employed. A DRI filter limit of ±2 degrees was needed to suppress the effect of the filter for large errors and improve the maneuver and acquisition response. Although this design has satisfactory in-the-large performance, the susceptibility of the system to extraneous noise and disturbances is increased due to the addition of the lead-lag filter and is of particular significance during the cruise mode since low gas consumption is desired. The effect of disturbances such as low-g slosh forces was not investigated with this design.

In the parallel DRI/lead-lag design, the lead-lag circuit deadzone is larger than for the DRI circuit and provides a fast responding control system during acquisitions and maneuvers. When the system is close to its steady-state condition, the DRI circuit provides fine pulsing control augmentation. During inertial hold and cruise modes, the DRI

circuit predominates in the limit cycle operation. The performance of the switched DRI/lead-lag, the series DRI/lead-lag, and the parallel DRI/lead-lag designs are comparable. The parallel DRI/lead-lag circuit is the preferred design since mode switching is eliminated altogether, redundancy is inherent in its design, and it is not as sensitive to extraneous noise or disturbances as the series design.

2. PERFORMANCE

2.1 Rigid Body Responses

Switched DRI. The responses for two DRI time constants (τ = 2 sec, τ = 50 sec) are presented in Figure E-7. The following characteristics can be observed from this figure:

- Separation. The larger time constant increases the time for nulling the rates as the DRI filter feedback prevents the gas jets from firing for a period proportional to the filter time constant.
- Sun acquisition. The use of the small time constant provides faster response. The gas usage is almost ideal for either time constant.
- Canopus acquisition. Faster response and better convergence is provided by the smaller τ. The gas usage is nearly ideal for either time constant.
- Maneuvers. With small τ, large gas usage and oscillatory response due to decreased rate damping resulted. Large τ produced large gyro error angles. For τ = 2 sec, the gas consumption relative to the ideal usage was increased by approximately 400 percent; for τ = 50 sec, the increase was about 40 percent.
- Cruise. Maximum attitude rates and excursions during the cruise mode are given in Table E-1. The values given are within prescribed mission requirements. τ equals 50 sec.

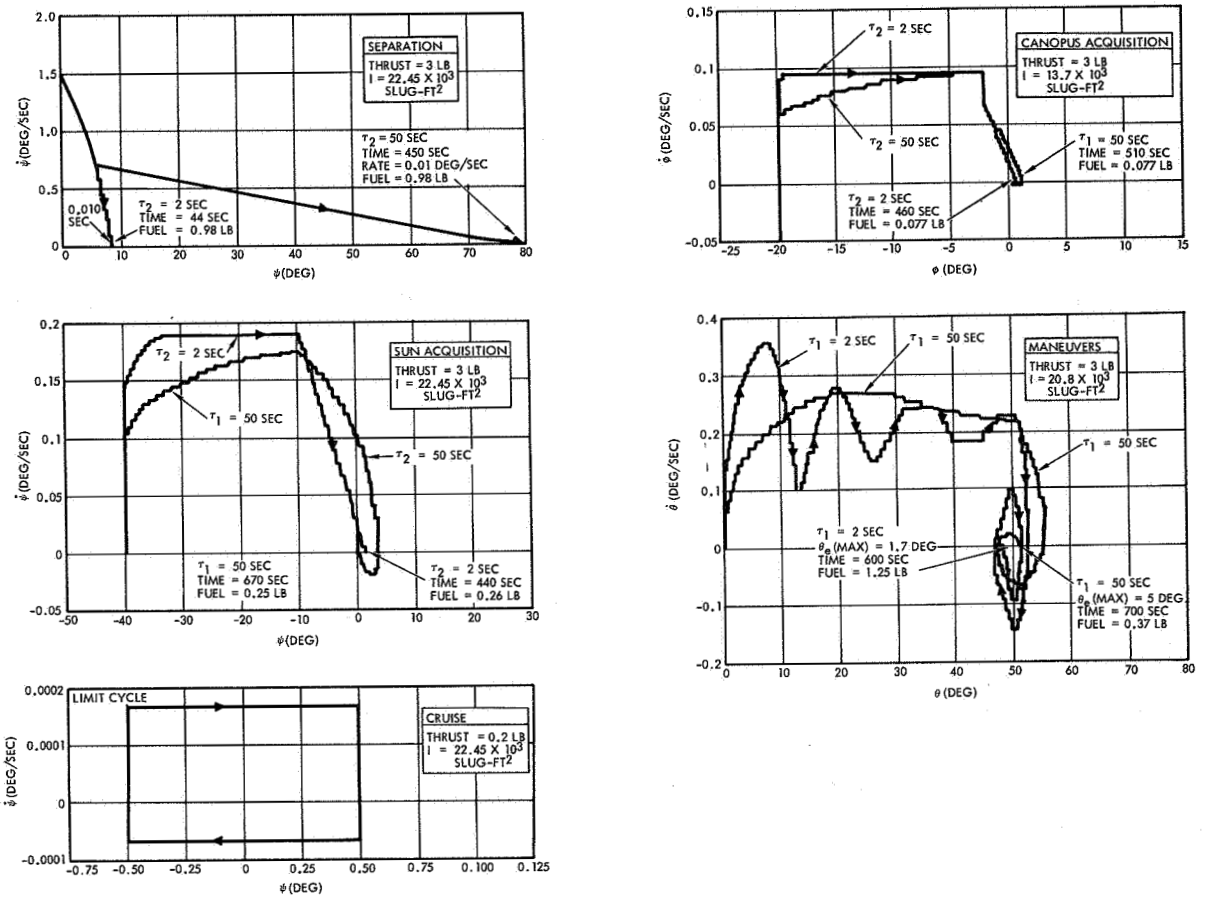


Figure E-7. Switched DRI Design Responses

Switched and Parallel DRI/Lead-Lag. The responses for the parallel DRI/lead-lag are essentially the same. The following observations can be made from the parallel DRI/lead-lag responses shown in Figure E-8.

- Separation. The rate nulling operation is accomplished rapidly with nearly ideal fuel consumption.
- Sun and Canopus acquisition. Responses were rapid and fuel usage almost ideal due to the absence of overshoots or oscillations in the response.
- Maneuvers. Response was rapid with almost ideal fuel usage. Maximum gyro error was 1.6 degrees during the maneuver.

Table E-1. Cruise Mode Rate and Attitude Errors

	Maximum Rates (deg/sec)		
Time of Flight	Yaw	Pitch	Roll
Trans Mars coast	2.75×10^{-4}	2.55×10^{-4}	4.2×10^{-4}
Mars orbit including planetary scan platform imaging	19.8×10^{-4}	12.6×10^{-4}	11.0×10^{-4}

	Maximum Attitude Error (deg)		
Time of Flight	Yaw	Pitch	Roll
All except planetary scan platform imaging	0.5	0.5	0.5
Planetary scan platform imaging	0.25	0.25	0.25

- Cruise. Cruise mode operation is dominated by the DRI circuit. Maximum attitude rate and excursions are given in Table E-1.

Series DRI/Lead-Lag. The following observations can be made from the series DRI/lead-lag responses shown in Figure E-9.

- Separation. The rate nulling operation is accomplished rapidly with the use of the two-degree limit on the DRI filter.
- Sun acquisition. The limit on the DRI filter enables a fast sun acquisition. Gas usage is near ideal since no overshoot occurs.
- Canopus acquisition. The DRI filter limit provides a near ideal response.

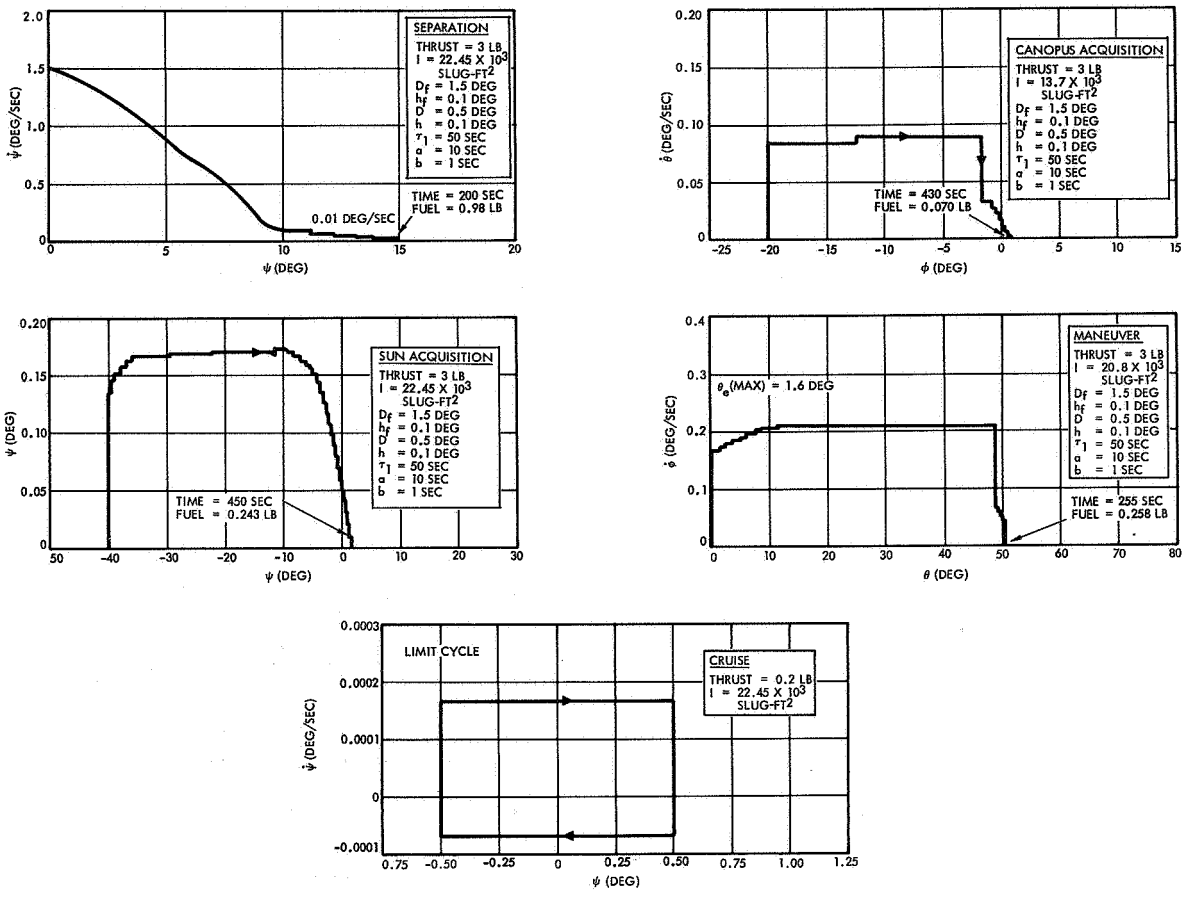


Figure E-8. Parallel DRI/Lead- Lag Design Responses

- Maneuvers. The lead-lag filter provides good damping and fast response for the maneuvers. The limit on the DRI filter suppresses its effect. Without the limit, a sluggish response would occur.

- Cruise. The cruise mode limit cycle characteristics are similar to those for the other designs except that the gas jets switch on a few millidegrees before the attitude deadband limits are reached due to the lead-lag filter. Sensitivity to system noise and disturbances are increased, however, due to the lead-lag filter.

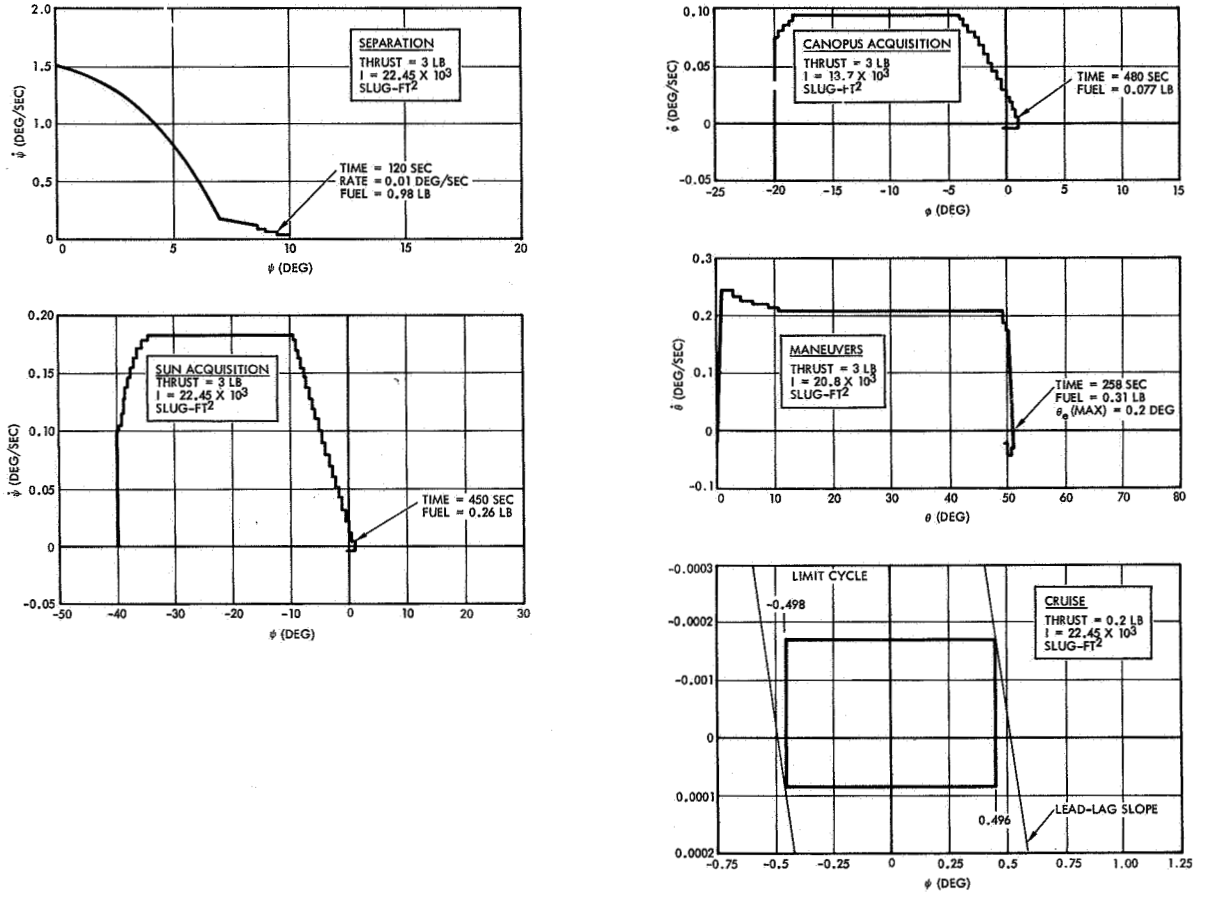


Figure E-9. Series DRI/Lead-Lag Design Responses

Time, Gas Consumption, and Maneuver Attitude Errors. A summary of the time and gas consumption for the various mode and circuit designs given previously are presented in Table E-2. The peak gyro error during maneuvers for nominal and a failed thrust condition are also given. The significant differences occur in the performance parameters for the maneuvers. The desirability of lead-lag compensation during maneuvers is clearly indicated and, hence, was included in the recommended design.

Table E-2. Comparison of Control System Performance Showing the Time and Gas Expended in Executing Modes and the Peak Gyro Error During Reorientation Maneuvers

Mode Completion Time (sec)

Mode	DRI with τ = 50 sec	DRI with τ = 2 sec	Parallel DRI/ Lead-Lag	Series DRI/ Lead-Lag with DRI Limits
Separation	450	44	200	120
Sun acquisition	670	440	450	450
Canopus acquisition	510	460	430	480
Maneuver	700	600	255	258

Gas Usage (lb)

Mode	DRI with τ = 50 sec	DRI with τ = 2 sec	Parallel DRI/ Lead-Lag	Series DRI/ Lead-Lag with DRI Limits
Separation	0.98	0.98	0.98	0.98
Sun acquisition	0.250	0.260	0.243	0.26
Canopus acquisition	0.077	0.077	0.070	0.077
Maneuver	0.37	1.25	0.258	0.31

Peak Gyro Error During Maneuver (deg)

Mode	DRI with τ = 50 sec	DRI with τ = 2 sec	Parallel DRI/ Lead-Lag	Series DRI/ Lead-Lag with DRI Limits
Nominal Thrust	5.0	1.7	1.6	0.2
One thruster failed	9.4	3.2	1.6	0.4

2.2 Low-G Slosh Effects

During the TRW Systems Task C studies, the effects of low-g (less than 10^{-4} g) propellant slosh during the cruise modes and the transition from powered flight to cruise were investigated. This investigation employed low-g propellant slosh models pertaining to the LM propellant tanks which were determined in the propellant hydrodynamic studies. In the control system analysis, extreme conditions such as large initial slosh mass displacements, zero damping in the slosh model, and an increase in the slosh effects by a factor of 10 were imposed. Moreover, the slosh mode frequency was varied, both with and without the effects of solar pressure torques, in an attempt to obtain a slosh instability. It was concluded that low-g propellant slosh effects are not deleterious to control system stability or performance and that additional gas would not be required to counteract these effects. It was also indicated in these studies that a large DRI time constant, such as 50 seconds, was desirable to reduce the possibility of inadvertent multiple gas jet pulsing. The use of lead-lag circuits or series DRI/lead-lag circuits, however, was not included in these investigations.

Although the recommended propellant tank configuration differs from those for the LM vehicle, the conclusions are still considered to be valid and pertinent since the differences are small. The slosh mode frequency is determined primarily by the spring constant associated with the fluid-vapor interface membrane and the slosh mode mass, hence is not expected to differ appreciably. The spring constant is dependent primarily upon the surface tension and capillary forces corresponding to a given fluid and tank geometry. Since a factor of 10 increase in slosh effects, made in the previous propellant slosh studies, was found to be of no consequence, it is considered safe to conclude that the recommended propellant tank configuration would also provide low-g slosh modes which are not deleterious to the DRI circuit cruise mode design.

2.3 Attitude Control Maneuver Errors

The three-sigma attitude control maneuver errors are presented in Table E-3; these values are used in the thrust vector control error budget under Section 2.2 and also in the determination of the capsule separation attitude errors. Assuming a capsule-to-spacecraft, three-sigma alignment error of 0.4 degree and using the values in the table, the three-sigma capsule separation error is 0.48 degree. With a control deadband of ±0.25 degree, the total capsule separation error is less than 0.73 degree, which is within the mission requirement.

The attitude errors resulting from the coast phase limit cycle would be nulled out during the powered flight phases by the linear thrust vector control system operation.

3. GAS REQUIREMENTS

The gas requirements for the recommended spacecraft design employing the parallel DRI/lead-lag circuit are shown in Table E-4. The total gas is contained in two supply systems. Each system supplies one-half of the control moment as illustrated in Figure E-10. A redundancy factor of three is employed to enable completion of the mission in the event that one valve fails in the open position. If a gas jet fails "on," such as is exemplified in the figure, jet valves 2 and 4 would turn on to combat the disturbance moment from jet 1. Valve 3 would remain closed. Since the control moment is twice as large as the disturbance moment, valves 2 and 4 would be on at a one-half duty cycle. The gas from system B will eventually deplete with two-thirds of the system B gas having been ported through valve 1 and one-third through valve 4. One-third of the gas from system A would also be expended in this failure operation. With this type of failure, two-thirds of the gas remaining in one system must suffice for the entire mission, hence, the redundancy factor of three.

Table E-3. Three-Sigma Attitude Control Maneuver Errors

Accuracy of optical sensors	0.1 degree
Gyro torquing error	0.2
Gyro alignment error	0.1
Gyro drift (0.1 deg/hr)	0.1
Attitude control limit cycle errors	0.05
Root-Sum Square	0.27 degree

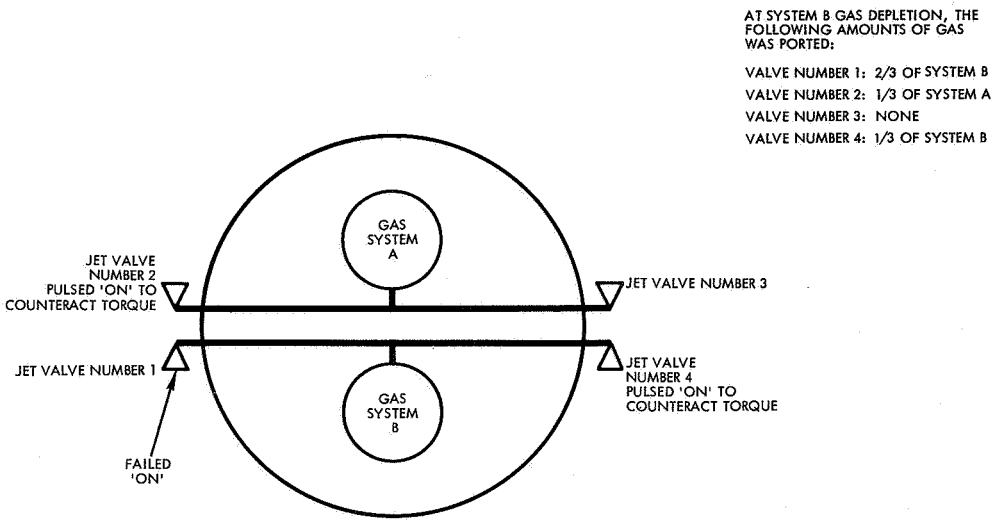


Figure E-10. Reaction Control System Operation in the Case of Failure of One of the Solenoid Valves in the "On" State

The gas requirements for the cruise mode include the use of thruster heaters to double the gas specific impulse to 120 seconds. The gas requirements for sun and Canopus acquisition and reorientation maneuvers were based upon six operations during the trans-Mars coast phase and four operations during Mars orbit coast.

The powered flight roll gas requirements were based upon a two foot-pound roll torque during the high-thrusting Mars orbit insertion phase and a 0.34 foot-pound roll torque during the low-thrust main engine phases. These values were assumed from experience in the past with vehicles employing a single main engine.

Table E-4. Voyager Reaction Control System Gas Requirements for the Recommended Spacecraft Employing Parallel DRI/Lead-Lag Circuit Designs

	Mode	Gas Consumption (lb)
1.	Initial rate nulling	1.26
2.	Cruise mode (with heaters)*	
	a. Mars transit	1.50
	b. Orbit	1.06
3.	Sun-Canopus acquisition (six times during Mars transit, four times during Mars orbit)	5.15
4.	Inertial and maneuver mode (six times during Mars transit, four times during Mars orbit)	5.18
5.	Capsule separation	0.73
6.	Powered flight roll	2.17
		17.05
	With redundance factor	x3
		51.15
	With 10 percent for contingencies	+5.12
		56.27
	With ullage	+2.60
		58.87
	With leakage	+2.20
	Total Gas Requirement	61.07 lb

*Without heaters, these values are doubled. With heaters and a 0.1-lb RCS low thrust level, these values are reduced to a total of 1.74 pounds.

APPENDIX F

POWERED FLIGHT CONTROL ANALYSIS

1. THRUST VECTOR POINTING ACCURACY

Thrust vector pointing accuracy is attained with the use of electronic integration of the control error signal. It was concluded that the use of devices such as lateral accelerometers would not be necessary or desirable for meeting accuracy requirements, particularly since the failure of these devices would further increase thrust vector point errors or produce control system instability.

Two types of feedback integration designs were considered, attitude feedback integration with and without engine angle feedback integration. The attitude plus engine angle integration feedback reduces the pointing error due to offsets between the center of gravity and thrust vector. The attitude integration feedback reduces the pointing error due to thrust vector angular misalignments. These designs are shown by the block diagram given in Figure F-1. Note that the engine angle loop is a positive feedback loop which would cause the engine to drift into its limits prior to the powered flight phase. Engine angle feedback, if employed, must be opened during nonthrusting engine phases.

Large radial offsets of the center of gravity from the vehicle centerline result primarily from the weight and location of the planetary scan platform. These offsets range between 2 and 3.5 inches during the Mars orbit insertion phase. Instead of employing attitude plus engine angle integration feedback to reduce the effect of these offsets, it is feasible to bias the control system such that the effects of predetermined or mean center of gravity offsets are removed. The

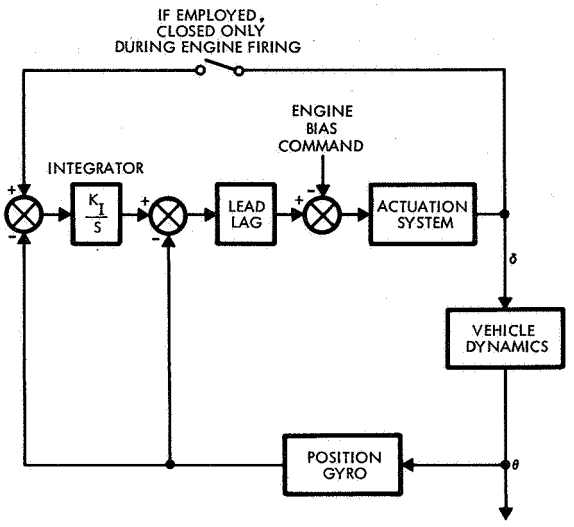


Figure F-1. Thrust Vector Control System with Electronic Integrator

diagrams shown in Figure F-2 illustrate the result. The engine axis can be commanded so that it passes through the vehicle mean center of gravity. The spacecraft can also be rotated, as part of the coast phase reorientation maneuver, such that the thrust vector points in the desired direction. With this implementation, the trajectory errors and the large transients on the vehicle due to nominal offsets are reduced. This technique is preferred as shown by the following considerations.

The magnitudes of the mean center of gravity angle are shown in Table F-1. These angles are large in the pitch axis due to the planetary scan platform. The Mars orbit trim angles shown are after capsule separation. The changes in the center of gravity offset angles result from movement of the vehicle center of gravity in the longitudinal as well as radial direction.

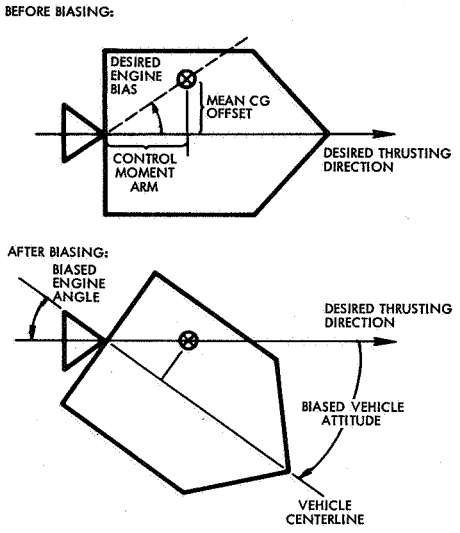


Figure F-2. Use of Spacecraft Rotation and Engine Bias Commands

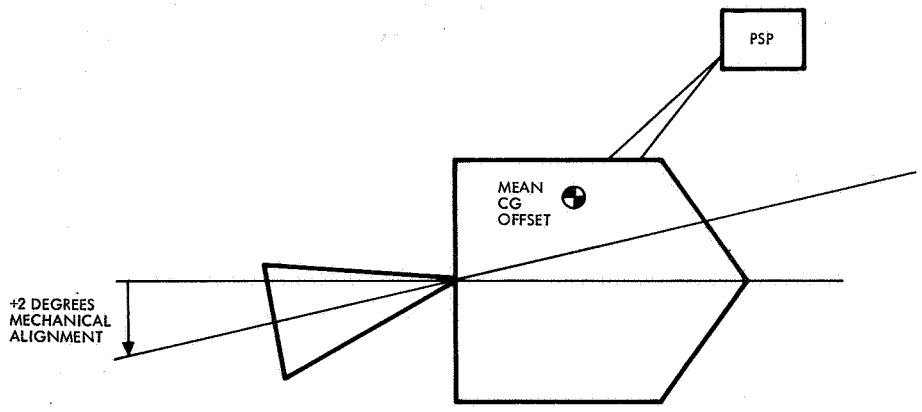
Table F-1. Mean Center of Gravity Offset Angles for the Start and End of the Three Powered Flight Phases

The angles defined by the ratio of the mean center of gravity offsets to the thrust vector control moment arm are:

	Mean Yaw Center of Gravity Offset Angle (deg)	Mean Pitch Center of Gravity Offset Angle (deg)
Midcourse corrections, start	0.112	1.77
Midcourse corrections, end	0.126	1.80
Mars orbit insertion, start	0.126	1.80
Mars orbit insertion, end	0.168	2.18
Mars orbit trim, start	0.585	5.3
Mars orbit trim, end	0.603	5.4

The mean center of gravity offset pitch angles are excessively large after capsule separation, with little engine deflection capability remaining. In order to increase the engine capability, it is recommended that the engine pitch axis be mechanically canted two degrees in the direction of the planetary scan platform as shown in Figure F-3. This produces an engine pitch gimballing range of -4 and +8 degrees relative to the vehicle centerline; this range is within the ±8 degree maximum engine gimballing space allotted in the spacecraft design. The engine excursions would be controlled through electronic limits in the engine command signal and engine mechanical stops. The minimum engine deflection capability, which occurs at the end of the Mars orbit trim firings, is 2.6 degrees after compensation for mean center of gravity offsets. With the absence of significant disturbances in Mars orbit, this deflection capability is considered sufficient for vehicle control. The spacecraft attitude is also rotated in pitch through the two-degree angle during the coast phase reorientation maneuver to aim the thrust vector in the desired direction. No mechanical bias angles are required in the yaw axis.

The mechanical bias reduces the electrical bias needed to trim the nominal center of gravity offsets. The desired electrical bias angles to remove the mean center of gravity offset effects with and without the mechanical engine alignment are shown in Table F-2. Since the changes in the mean center of gravity offset angles are small during a firing phase, constant biases within each phase are sufficient.



ENGINE PITCH ANGLES RELATIVE TO SPACECRAFT CENTERLINE IS 2±6 DEGREES.

Figure F-3. Desirable Mechanical Pitch Angle Alignment of the Engine

Table F-2. Desired Engine Electrical Bias Angles to Remove Mean Center of Gravity Offset Effects During the Three Powered Flight Phases

	Desired Electrical Yaw Bias Angle (deg)	Without Mechanical Alignment, Desired Electrical Pitch Bias Angle (deg)	With Mechanical Alignment, Desired Electrical Pitch Bias Angle (deg)
Midcourse corrections	0.121	1.79	-0.21
Mars orbit insertion	0.154	2.05	0.05
Mars orbit trim	0.597	5.37	3.37

The total steady-state thrust vector pointing errors resulting with the various compensations are shown in Table F-3. The three-sigma errors from the attitude reorientation maneuver (0.27 degree given in Volume 2 Appendix E, Table E-3) were included in these results. The desirability of integrators is apparent. The use of attitude integration feedback with biases appears more desirable than attitude plus engine angle integration.

2. THRUST VECTOR CONTROL SYSTEM STABILITY

The thrust vector control system for the recommended vehicle configuration, with or without the capsule, has stable powered flight propellant slosh modes due to the inherently stable slosh geometry. This geometry is obtained for a spherical tank by maintaining the longitudinal center of gravity of the vehicle forward of the propellant tank center.

An example of control system stability is given by the gain-phase plot shown in Figure F-4, corresponding to the pitch plane at the start of Mars orbit insertion. A lead-lag filter is included for damping with a lead at 1 rad/sec and a lag at 20 rad/sec. An attitude integration feedback loop is included and results in the low-frequency phase crossover at 0.4 rad/sec. The selected integrator gain of 0.125 is quite acceptable and results in a low-frequency rigid body gain margin of 22 db. The rigid body phase margin is 38 degrees. The two bus

Table F-3. Steady-State TVC Pointing Errors in Degrees (Three-Sigma)

	No Integrators	Attitude and Engine Angle Integration	Attitude Integration Without Center of Gravity Angle Bias	Attitude Integration With Center of Gravity Angle Bias (Recommended Design)
Midcourse correction				
Yaw	0.815	0.570	0.548	0.428
Pitch	2.915	0.570	2.218	0.428
Mars orbit insertion				
Yaw	1.017	0.570	0.540	0.393
Pitch	4.723	0.570	2.393	0.393
Mars orbit trim				
Yaw	1.153	0.570	0.834	0.400
Pitch	2.314	0.570	1.750	0.400

These values include the steady-state effects of a 3σ center of gravity offset uncertainty (0.25 inch), misalignment angle (0.5 degree), and a three-sigma thrust vector offset (0.25 inch). They also include the following g-sensitive gyro drift errors based upon a 0.7-degree-per-hour-per-g drift.

Midcourse correction	0.003 degree
Mars orbit insertion	0.042 degree
Mars orbit trim	0.000 degree

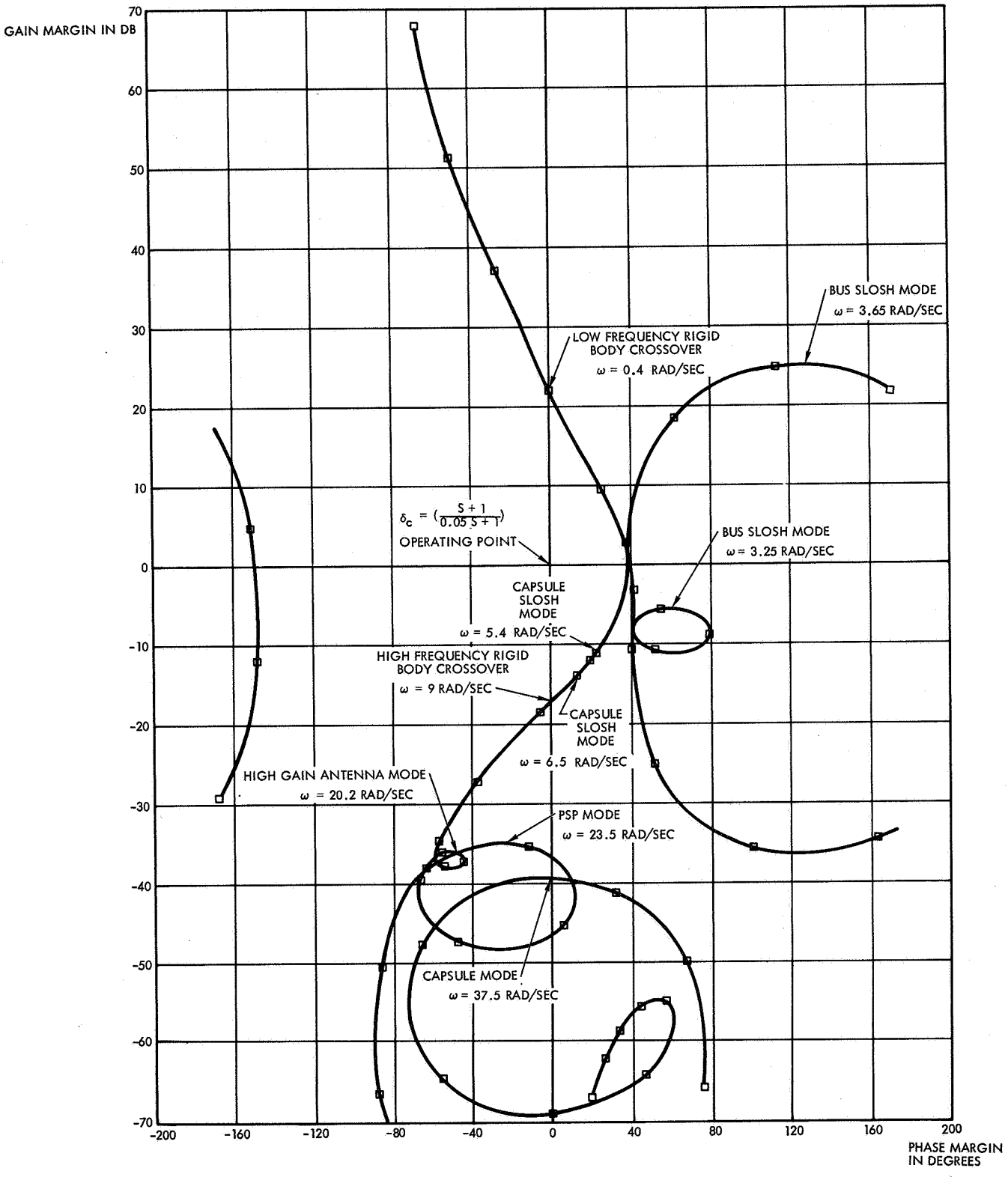


Figure F-4. Powered Flight Gain and Phase Stability Margins

slosh modes are stable at 3.65 and 3.25 rad/sec. The capsule slosh modes are negligible. The high-frequency rigid body crossover occurs at 9 rad/sec with a gain margin of 17 db. The high-gain antenna bending mode at 20.2 rad/sec has a gain margin of 36 db. The planetary scan platform mode at 23.5 rad/sec has a gain margin at 35 db. The capsule mode at 37.5 rad/sec shows a 39.5-db gain margin. Note that the primary bending modes result from the flexing of the large appendages. The bus body acts essentially as a rigid body in these modes; hence, stability is independent of the location of the gyro package along the spacecraft body.

APPENDIX G

C-1 ENGINE CONTROL

With the use of C-1 engines for backup powered flight operations, the following three attitude control system designs for pitch and yaw control were considered:

- Pulsing of the C-1 engines
- Use of existing or upgraded gas jets
- Gimballing of the C-1 engines.

Roll Control is maintained with the gas jet system.

1. PULSED C-1 ENGINE ATTITUDE CONTROL

The recommended attitude control is the pulsed C-1 engine design. The C-1 engines are mounted on axes 40 degrees from the pitch and yaw attitude control axes and in line with the engine actuators as shown in Figure G-1. Because of this, the engine actuator command signals can be conveniently employed as commands to the C-1 engines. The addition of "minimum off-time" switching circuits are required to obtain the desirable pulsing operation with these engines. A block diagram of the signal routing to the C-1 engines is shown in Figure G-2. Included in the minimum off-time switching circuits are the command reversing logic required to pulse "off" the appropriate engine as represented by the inverted deadzone switching circuit. Figure G-3 illustrates the desired pulsing. If the disturbance torque acts in a counterclockwise direction as shown, the attitude control system would command engines 3 and 4 "off." The duty cycle for engines 3 and 4 with a four inch c. g. offset is also shown in the figure.

The spacecraft c. g. offsets are large, and frequent pulsing "off" of the engines to counteract the associated disturbance torques is necessary. This frequent pulsing of the engines is not desirable since it reduces the net axial acceleration and efficiency of the orbit insertion firing. A longer thrusting duration would be required and increased velocity errors may result from the frequent pulsing. The velocity

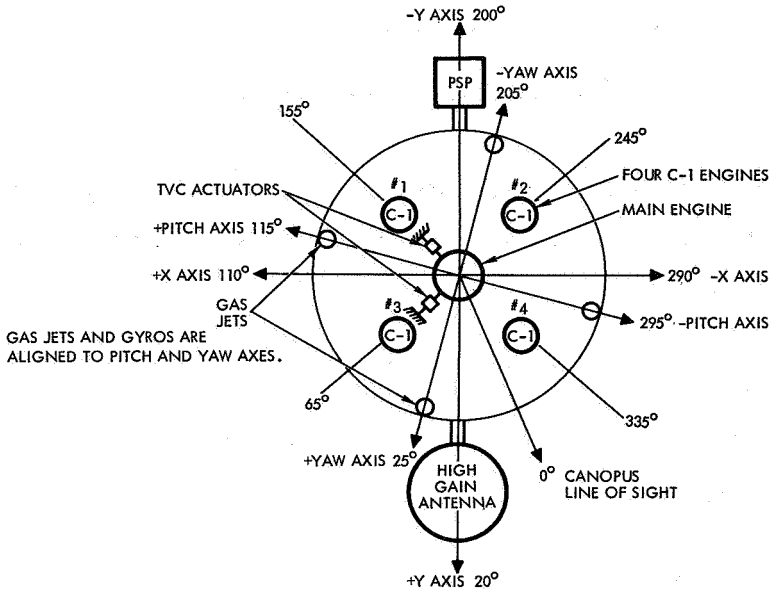


Figure G-1. Location of C-1 Engines Relative to Pitch and Yaw Control Axes

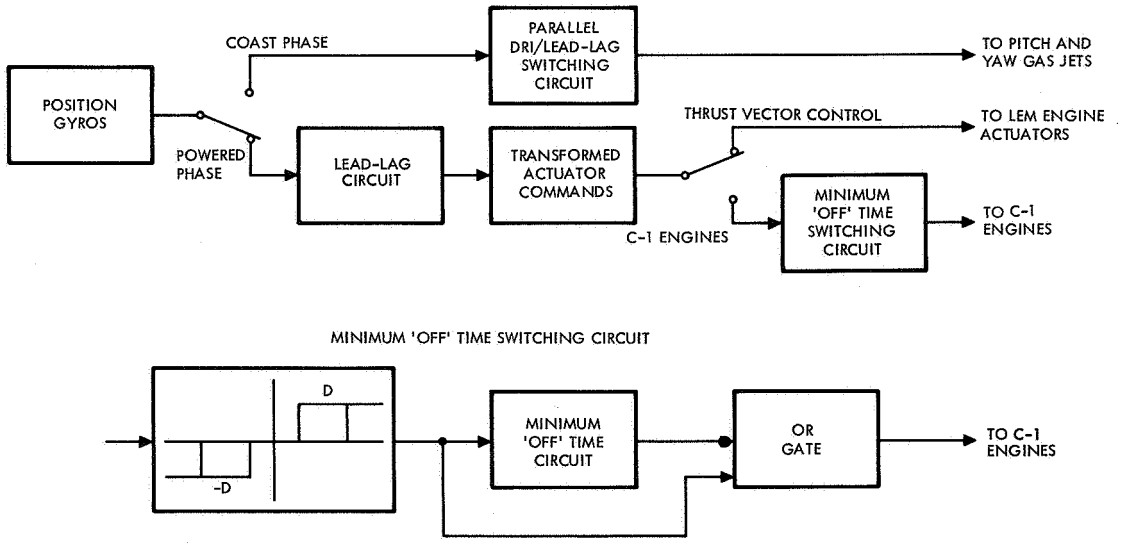


Figure G-2. Recommended Pulsed C-1 Engine for Pitch/Yaw Control

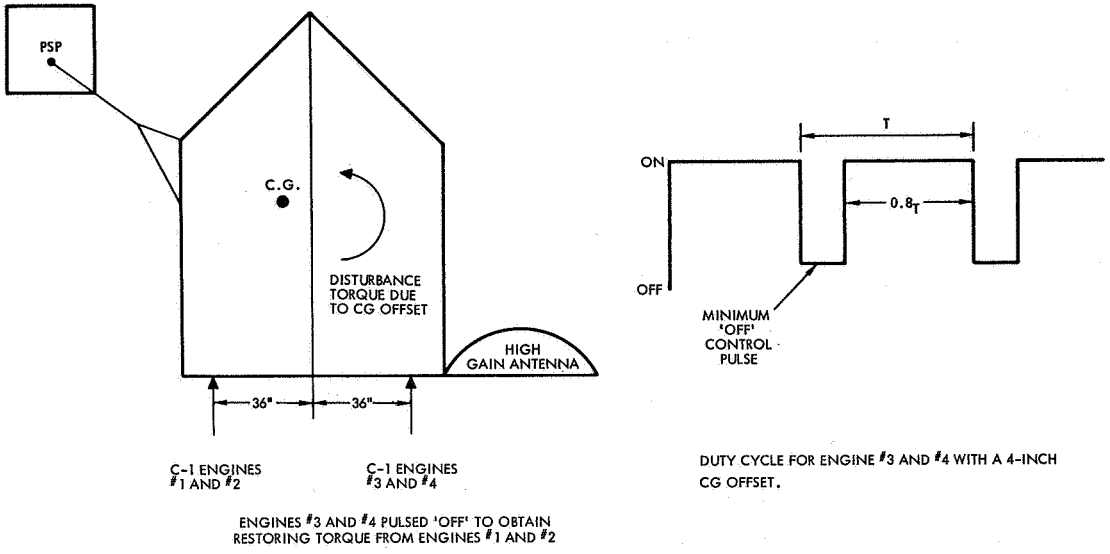


Figure G-3. Desired Pulsing of the C-1 Engines

errors are of particular importance during the Mars orbit insertion phase since only one firing for orbit insertion is made. The midcourse correction and Mars orbit trim phases are comprised of multiple firings so that velocity errors accrued in one firing can be compensated in subsequent firings. Therefore, it is recommended that the C-1 engines be mechanically canted approximately two degrees in order to reduce the mean c. g. offset and engine pulsing effects during the Mars orbit insertion phase. With this alignment, the duty cycle of the pulsing engines are expected to be greater than 99 percent "on" and less than one percent "off"; hence, its effect on axial acceleration and total firing time will be less than 0. 5 percent, an acceptable level. Without the two degrees of mechanical bias, the duty cycle would vary considerably (89 to 82 percent "on") during the orbit insertion phase and a reduction in axial acceleration by as much as 9 percent may occur.

The average duty cycle of the pulsing engine and the effective axial acceleration are given in Table G-1 for the different mission phases. Since the C-1 engines are aligned for Mars orbit insertion, the c.g. offset effects during the Mars orbit trim firings without capsule are appreciable with a duty cycle approximately 8 percent would be required for these firings. Since small changes in spacecraft velocity are made during these firings and since multiple firings are contemplated, the velocity errors are expected to be acceptable.

During the Mars orbit trim firings, if the minimum off-time circuit is set for a firing duration of 0.1 second, the frequency of the duty cycle would be 1.25 pulses per second. At a 0.2 second firing duration, this pulse rate would be reduced to 0.63 pulse per second. The limit cycle parameters are listed in Table G-2. The selection of the minimum "off" duration should be made in accordance with reliable engine pulsing operation.

The pulsing of the C-1 engine will, to a certain extent, excite the appendage flexural modes and propellant slosh modes. Although this is not expected to cause control system stability problems, simulation studies and further investigation of this operation is recommended.

Table G-1. Duty Cycle of Pulsed C-1 Engines and Effective Axial Acceleration Due to Mean Center of Gravity Offsets After Incorporating a Two-Degree Mechanical Alignment

	Duty Cycle of Pulsed C-1 Engines (percent)		Effective Axial Acceleration From Nominal (percent)
	On	Off	
Midcourse correction	98.8	1.2	99.4
Mars orbit insertion	99.32	0.68	99.7
Mars orbit trim, with capsule	98.4	1.6	99.2
Mars orbit trim, without capsule	84	16	92

Table G-2. Limit Cycle Parameters During Pulsed C-1 Engine Operation Due to Mean Center of Gravity Offset Effects. Minimum Pulse Durations of 0.1 and 0.2-Second Considered. *

	Maximum Angular Rates		Number of Pulses Per Second	
	T = 0.1 sec	T = 0.2 sec	T = 0.1 sec	T = 0.2 sec
Midcourse correction	0.123 deg/sec	0.246 deg/sec	0.12	0.06
Mars orbit insertion	0.170 deg/sec	0.340 deg/sec	0.064	0.032
Mars orbit trim, without capsule	0.510 deg/sec	1.02 deg/sec	1.25	0.63

*Angular excursions during limit cycle are within the ±0.5 degree deadzone.

2. GAS JET ATTITUDE CONTROL

Use of the coast phase gas jets for attitude control during the C-1 engine operation is not recommended due to excessive gas requirements and large control moment requirements. Even if a mechanical alignment angle of two degrees is employed to reduce mean center of gravity offset effects, a gas requirement of 212 pounds would result from movement of the center of gravity. The center of gravity offset dirturbance torque with this alignment angle would be 102 foot-pounds. The control moment required would be a minimum of twice this value or 204 foot-pounds, which is considered too large for upgrading of the two-level gas jet design; therefore, an additional set of valves and jets would be required. If the bias angle is increased to 3.6 degrees, the disturbance torque would be reduced to 54 foot-pounds; however, the corresponding gas requirement is increased to 1298 pounds, which is an intolerable level. Use of the gas jets, therefore, does not appear to be appropriate.

3. GIMBALLED C-1 ENGINE THRUST VECTOR CONTROL

The use of gimballed C-1 engines for control of the vehicle is not recommended due to the complexity and additional hardware required for actuation of these engines.

The additional electrical bias angles for trajectory correction and the C-1 engine gimballing actuators required for this design are not considered justifiable in view of the satisfactory attitude control performance that most certainly can be achieved with the pulsed C-1 engine design.

APPENDIX H

INERTIAL REFERENCE UNIT TRADEOFFS

In the course of selecting the preferred design for the inertial reference unit, a number of alternate instruments and loop configurations were considered. This section briefly describes these designs along the reasons for selecting the recommended design.

1. ALTERNATE GYROS

Four gas-bearing gyros were considered for Voyager. The list was limited to units equipped with gas spin bearings because of the increasing evidence indicating that this type unit is more reliable than ball bearing designs. The units considered are listed in Table H-1. All of these gyros exhibit performance compatible with the Voyager requirements. In addition, since some of the units are physically smaller and require less spin motor power, savings in size, weight, and power could be realized by utilizing units other than the recommended GI-T2-D.

As stated previously, the overriding consideration in selecting this gyro instead of one of the others was based on greater confidence in the unit. The large production and field experience of the GI-T1-B, which, except for minor modifications, is identical to the GI-T2-D, and the large amount of gyro operating time support the argument that this gyro has the greatest potential of being the most reliable unit. In addition, this gas bearing has operated successfully in a zero-g space environment, a condition to which the other candidate gyros have not yet been subjected. Future manufacturing and field experience may substantiate the reliability of a smaller gyro at which time such a unit could be considered in the design.

Table H-1. Candidate Gyros for Voyager Spacecraft

Manufacturer and Gyro	Approximate Quantity Built	Programs Where Units Have Been Utilized	Size Diameter x Length (in.)	Weight (lb)	Spin Motor Power (w)	Comments
Nortronics GI-T2-D	850*	Minuteman 2* Minuteman 3 Mark IV SINS	3.5 x 5.0	3.5	6.5	*These items refer to the GI-T1-B which is the same basic design as the GI-T2-D
Nortronics GI-K7-G	50	C5A Navigation System	1.7 x 3.0	0.6	5.0	
Honeywell 334C	15	-	2.0 x 3.5	1.0	3.0	
Kearfott King II	10	-	2.0 x 3.1	1.0	6.5	

2. ALTERNATE GYRO LOOP CONFIGURATIONS

Four additional loop configurations utilizing single-degree-of-freedom gyros were considered. These loops differ primarily in the manner in which the angular position information is obtained.

Rate Loop With an Integrating Capacitor in Series with the Torquer. This loop has been utilized in some previous space missions. However, the integrating capacitors exhibit hysteresis and leakage characteristics that contribute to gyro drift.

Rate Loop Coupled to a Voltage to Frequency Converter and Accumulator. This configuration integrates angular rate by counting the voltage-to-frequency converter output. Since the recommended Voyager guidance and control system is analog, the accumulator output must be converted to an analog signal for processing. The result is that this mechanization has a relatively high parts count and hence was discarded because of low reliability.

Rate Loop With Operational Amplifier Integrator. This configuration utilizes an integrator consisting of an operational amplifier with a capacitor feedback circuit. The major difficulty with this loop is that the parts count is higher than that of the selected design and hence it is not as reliable. Another problem is that the long-term amplifier bias instability would result in drifts which are inconsistent with Voyager requirements.

Pulse Torqued Gyro. This loop is similar to that of the proposed accelerometer design. As with the voltage-to-frequency converter configuration, the output of this loop is a pulse frequency proportional to input angular rate. An analog angular position signal is obtained by accumulating and digital-to-analog converting as before. The relatively high parts count is again a problem which results in a less reliable assembly. This mechanization would undoubtedly be given further

consideration if the guidance and control system were controlled by means of a digital computer. In this case, the output is in digital form, and the accumulator and digital-to-analog converter are not required. Also, the VSA loop could also easily interface with a computer.

3. ALTERNATE ACCELEROMETERS

The Bell Model VII and Honeywell GG177 flexure supported accelerometers were considered for this application. While their performance is comparable to the Kearfott 2401, their manufacturing and field experience is considerably less. Also, because of the longer availability of the 2401, a great amount of long-term scale factor and bias stability data exists (some extending over a four-year period), which permits more confidence in the accelerometer performance over the Voyager flight time.

4. ALTERNATE ACCELEROMETER LOOP

An alternate configuration was considered which consists of an analog rebalance loop coupled to a voltage-to-frequency converter. This design was discarded because it is less reliable, a conclusion which results from its increased circuit complexity. The voltage-to-frequency converter bias also tends to increase the overall bias uncertainty, which is undesirable because this effect is the dominant error in the velocity measurement during the mid-course velocity correction maneuvers. The accelerometer bias uncertainties associated with the preferred design presently cause this error to be at its maximum practical limit for the Voyager application.

5. ACCELEROMETER PACKAGES

Three velocity measurement packages were investigated for possible use on Voyager. Each is a single-axis package with self-contained electronics that produce an output pulse train with a frequency proportional to input acceleration. The three units are:

- Bell DVMIIA
- Honeywell GG386
- Arma D4e System

The first two are conventional units utilizing the Bell Mod VII B and GG179 accelerometers, respectively. The Arma unit is a vibrating string accelerometer which produces an output frequency proportional to input acceleration. However, its output is produced directly by the sensor without the use of pulse rebalance loops or voltage-to-frequency converters. While this initially seemed a very simple mechanization, further investigation revealed the requirement for a bias correction circuit which automatically compensates for the bias creep (2 micro g/day) and temperature sensitivity (20 micro g/^{o}F). The resulting system is not materially different in overall complexity from the others.

In the Voyager design, the weight and power advantages and alignment simplification realized by combining the gyro and accelerometer functions in a single assembly were the deciding factors in not utilizing these packages.

6. ADDITIONAL FAILURE DETECTION METHODS

Failure of the inertial reference unit during either the reorientation or engine thrust periods could have very serious consequences in the Voyager mission. This is especially true during Mars orbit insertion. Of course, the particular inertial reference unit selected to serve as the guidance and control system reference during these maneuvers will be self-tested through the command and data telemetry channels prior to each maneuver. Having checked out positively immediately prior to use, the probability of failure during a (typical) two-hour maneuver is admittedly very small, but nonetheless not zero. Because of this situation a preliminary study was conducted to determine if the two inertial reference units operated simultaneously and with interconnecting logic could be arranged so as to automatically switch from the controlling assembly to the alternate during these maneuvers in the event of a single failure in the first unit. A "voting" technique of failure detection is not feasible here since only two assemblies are planned for installation on the Voyager spacecraft. Therefore, the problem reduces to designing a system of logic which will switch from the controlling assembly to the redundant unit provided that the detected failure was really in the controlling

assembly and not vice versa. Note that this capability is only required during the gyro position operating modes. A list of the major failure possibilities is given in Table H-2.

Table H-2. Major Failure Modes in Inertial Reference Unit

Failure	Comment
Wheel stops	This would be detected by the spin motor rotation detector circuit which operates continuously when the assembly is energized.
Temperature control fails	This would be monitored continuously by housekeeping telemetry.
Torquer circuit fails	
	Torquer current too high or present when not commanded
	Torquer current too low
Pickoff circuit fails	
	Pickoff output too high (typically a saturation value)
	Pickoff output too low (typically zero)
Excessive gyro gimbal stiction	
Accelerometer failure	

First consider a single failure in the gyro portion of the assembly. A simple scheme can be implemented which will detect a failure that occurs in the controlling unit (the unit whose gyro outputs are being servoed to null by the remainder of the guidance and control subsystem). If both units, each having been self-checked immediately prior to use, are operated and commanded simultaneously, they will track each other in output except for errors caused by small differences in drift coefficients and torquing rates. This is true even though the redundant unit is not being servoed to null, since it receives the same angular inputs as the controlling unit. Then, given that the above failure condition is met, a voltage on the redundant output which exceeds a certain absolute value

could be utilized to indicate a failure in the controlling unit. The decision value would be selected based on the three-sigma drift and torquing tolerances. Then by switching to the redundant package, the maneuver could be salvaged with very little degradation.

The difficulty with this scheme arises, of course, when the failure occurs in the redundant unit. A number of the failures listed in Table H-2 can lead to a high redundant output voltage which would subvert the intent of the above logic rule and cause the system to switch to the failed unit. The probability of the occurrence of this situation can be reduced by the addition of continuous self-test circuitry, similar to the spin motor rotation detection system, which would operate during the maneuvers. Examination of the failure list reveals that the most troublesome failures are those which occur in the torquing circuit. For instance, if the redundant unit torques at the wrong angular rate or at the wrong time, a large output signal can occur. Therefore, a circuit designed to check the torquer current entering (and perhaps leaving) the gyro to determine that it is within some tolerance of the correct value could be utilized to determine that the proper torquer current was applied during the correct time interval. The measurement tolerance on the current monitoring circuit need not be as small as the current source output specification, because current source and torquer failures are most likely to be catastrophic, i.e., either a large current determined by the current source supply or zero output. If such a failure is detected in the redundant unit, the signal switching logic would be disabled. Also, if such a failure were detected in the controlling unit, this would be justification for an immediate switch to the redundant unit.

A high pickoff circuit failure would most likely be caused by a shorted output transistor. In this case, a plus or minus output voltage directly related to the supply voltage would appear on the output. This can be avoided if the redundant output comparator circuit is designed to reject the redundant output if it is higher than some preselected value as well as lower than the first limit, which was discussed previously. Note that these limits refer to the absolute value of the output, i.e., are applicable to both positive and negative position voltages. Note also that

a low pickoff failure would not be detected by the logic scheme and also that float stiction is not likely to be a problem as this type of failure would not cause the redundant output to change.

Failures in either of the accelerometer portions of the units can most readily be handled by means of a modified voting technique, where the third comparison is obtained by calculating the expected velocity change with time, based on estimates of engine thrust and spacecraft mass. In operation, this system would accumulate both velocity outputs into separate registers. At a point in time near the end of the engine burn period, the two outputs would be individually compared with a predicted value. The accelerometer whose output was closest to the predicted value would be selected to determine engine shutdown. An acceptable tolerance would be associated with this comparison and both accelerometer outputs could be rejected if both of their comparisons exceeded this tolerance. In this case, a time burn period would be utilized instead. Thus, in the worst case, i.e., two accelerometer failures, the velocity error would not exceed that which could be determined by the burn timing method.

The implementation of the comparators and the logic circuitry has not been studied in this analysis. It is expected that this circuitry can be made very reliable compared to the instruments and their loop electronics. Once the implementation is completed, further study must be devoted to consideration of logic failures and their effect on system performance.

APPENDIX J

OPTICAL SENSORS TRADEOFF

1. COARSE SUN SENSOR

Three approaches were considered before arriving at the recommended configuration for the coarse sun sensor. Only the recommended design is suitable for the upgraded spacecraft.

The recommended coarse sun sensor for the Voyager Task B study used four immersed silicon photovoltaic cells. Its output signal was derived in the same manner as the recommended design. However, because of the new recommended spacecraft appendages, no mounting locations are available with the required field of view for all four cells. Although the required field of view could be theoretically obtained by using sun shades, shading would destroy the most important advantages of immersed cells, which is their large field of view (greater than 2π steradians).

The second design considered employs five flat silicon photovoltaic cells (one is redundant with one of the remaining four) mounted in three locations on the periphery of the solar array panel. The pitch and yaw signals are obtained by adding and subtracting signals in the same manner recommended for the fine sun sensor. This requires more complex amplifiers than does the recommended coarse sun sensor. Because there is cross coupling of cells, an error in one axis also appears as an error in the other axis, even if no error in that axis exists. The best location of the five cells requires sun shades to prevent unwanted reflected light and to define the three fields of view. Three 6 x 12 inch shades, and seven 2 x 4 inch shades would be needed – all different. It is possible to make identical shades for the two assemblies of the recommended design.

2. FINE SUN SENSOR

Alternative sensors with the required null accuracy were obtained: the Bendix 1818823 and 1818874, and the Ball Brothers SS-100 array. On the basis of available information, these sensors have been discarded in favor of the recommended design. The Bendix 1818823 and 1818874 provide nonlinear monotonic signals which do not satisfy the 10-degree linear field-of-view requirement which prevents confusion of the sensor by the Earth's albedo. The Ball Brothers SS-100 array utilizes four FE-5A fine eyes and provides a five-degree linear region in a nominal 15-degree field of view. This is basically a quad-cell system employing four separate cells, each with a lens. It is difficult to match the response of four separate cells as well as the quadrants of a quad cell can be matched. In addition, the lens system alters the output characteristic from the nominal quad cell function. Thus, it would be more difficult to switch from coarse to fine sensors with small signal discontinuities.

A quad cell fine sun sensor is being developed at TRW. Data obtained so far indicates that 0.1-degree null accuracy is attainable.

3. CANOPUS SENSOR

Several makes of Canopus sensor are available:

- JPL/Barnes
- Santa Barbara Research Center (Hughes)
- ITT Federal Laboratories
- TRW Systems.

The Santa Barbara Research Center is a mechanically scanned and mechanically gimballed tracker with a limited lifetime and therefore unsuitable for the Voyager mission. Table J-1 lists the physical and performance characteristics of the remaining three sensors.

Table J-1. Characteristics of Candidate Canopus Sensors

Performance Parameter	ITTFL	JPL/Barnes	TRW
Instantaneous field of view	1 x 18 deg	0.85 x 11 deg	1 x 1 deg
Acquisition field of view	8.2 x 18 deg	4 x 11 deg	4 x 30 deg
Linear range in roll	±5 deg	±0.85 deg	±2 deg
Equivalent noise angle	15 arc. sec. rms	72 arc. sec. rms	12 arc. sec rms
Roll error gradient	1 v/deg	8 v/deg	4 v/deg
Time constant	0.19 sec	0.5 sec	0.25 sec
Stability of roll error gradient	±10 percent	±20 percent	±5 percent
Null stability	±4 arc. min.	±7.5 arc. min	±2 arc. min
Sun shutter	Focal plane	External	Focal plane
Size	4 x 5.5 x 12 inches	4 x 5 x 11 inches	4 x 5 x 12 inches
Power	21v, 2.85w 31v, 5 w	2400 Hz - 50 vrms 1.5w (does not include sun shutter power)	24-32v - 6w

The ITT Federal Laboratories tracker was designed for a 45-day mission and needs mechanical adjustment for launch date. This makes it unsuitable for the Voyager program, except with some redesign.

The JPL/Barnes sensor was designed for the Mariner C spacecraft and has been updated for the Mariner 1969. However, the exclusion field of view of 40 x 60-degrees greatly hinders its usefulness for Voyager.

The TRW Canopus sensor was designed by the same personnel that designed the Lunar Orbiter Canopus Sensor and represents a significant advance in versatility and sophistication.

3.1 Glare, Glint, and Mars Shine

Any Canopus sensor is subject to sun glinting from spacecraft protrusions in front of it. In the ITT Federal Laboratories and JPL/Barnes sensors, the single-axis slit configuration gives a video signal from lit baffle edges which is indistinguishable from the video signal from Canopus. TRW, at the beginning of its design effort, set out to eliminate this problem. By making the sensor closed loop in both axes, a smaller instantaneous field of view is possible. The cross scan deflection pattern reduces the video content from a baffle edge. Thus, the video signal content for a baffle edge is half that of the video signal from a star. Since the instantaneous field of view is smaller, the amount of incident energy which provides video is much smaller to start with. This reduces not only the glint problem but also reduces the overall background irradiance and makes it more difficult for stray particles to cause the sensor to lose Canopus, such as has happened with Mariner 4.

3.2 Other Advantages of TRW Sensor

By providing closed-loop tracking of the star image on the photocathode in both axes, it is possible to use the sun-spacecraft-star angle for verification of Canopus recognition.

The JPL/Barnes sensor uses an electrostatic dissector, and to provide the pitch electronic gimballing calls for high-voltage circuits to the deflections electrodes. For this purpose, a relay counter circuit is utilized. The TRW closed-loop approach with the magnetic dissector maintains contact automatically with Canopus and does not need mechanical relays.

Also, the construction of the CBS tube as used in the JPL/Barnes sensor makes it impossible to align the two axes perfectly, and cross coupling has to be employed to correct this over a limited range. The deflection coils of the F4012 used in the TRW design are adjustable and provide accurate alignment of the roll and pitch axis.

4. LIMB AND TERMINATOR DETECTOR

A performance summary of various candidate sensors is shown in Table J-2. The recommended design differs from the Task B design in that two optical systems are used to cover the ±50 degree field of view. The brightness in the image plane for images near the 50 degrees edge of the field, for the Task B design, would be about 20 percent of the brightness that it would be at zero degree. By limiting the field of each lens to ±25 degrees, the $\cos^4\theta$ attenuation would be for less. Significant variations in sensitivity over the field of view should be avoided due to the resulting error spread.

An alternate approach proposed by the Kollsman Co. uses seven small telescopes and seven detectors to cover a 75-degree field of view. The complexity of the processing circuitry is increased to handle all of these separate channels, but the need for all this complication does not appear justified.

Table J-2. Tradeoff Matrix for Limb and Terminator Crossing Detector

Parameter	Recommended Design	Voyager Task B Design	Kollsman Design
Optics	(2) 35 mm f/2	(1) 57 mm f/1.5	(7) 25.4 mm f/5
Field of view	100 x 2 deg	90 x 2 deg	75 x 1.5 deg
Spectral band (microns)	0.45 to 0.7	0.4 to 0.7	0.4 to 0.7
Size (each)	4 x 1.5 x 2.5 in.	6 x 1.75 x 4 in.	3.5 x 2 x 2.5 in.
Weight (each)	0.6 lb	0.6 lb	Unknown
Power (each)	0.2 w	0.2 w	Unknown
Amplifiers (each)	2	2	0
FET gates (each)	0	0	>15
Claimed accuracy	±1.0 deg	±0.7 deg	±1.0 deg

APPENDIX K

REACTION CONTROL TRADEOFFS

For attitude control purposes, many reaction control systems can be considered. The following list indicates the variety of systems available:

- Solid propellant systems
  1) Subliming solid
  2) Subliming solid bipropellant
  3) Cap pistol
- Liquid propellant systems
  1) Vaporizing liquid
     i. H_2O
     ii. NH_3
  2) Vaporizing liquid bipropellants
  3) Monopropellants
     i. N_2H_4
     ii. H_2O_2
  4) Hydrazine - plenum
  5) Liquid bipropellants
- Gaseous propellants
  1) Cold gas - nitrogen
  2) Resistance heated cold gas
  3) Isotope heated cold gas
  4) Gaseous bipropellants

- Electro-chemical
  1) Water electrolysis
  2) Solid propellant electrical - detonation thrusters (SPET).

Although the list looks formidable, the task of selecting a system for the Voyager mission is simplified by the fact that some of these systems cannot meet the system requirements. For example, the subliming solid, the vaporizing liquid, and the SPET systems are not capable of meeting the 3.0-pound thrust requirements. Furthermore, the bipropellant systems (subliming solid, vaporizing liquid, liquid, and gaseous) are not competitive because of the increased complexity required to control two fluids. The "cap pistol" approach, which consists of small solid propellant charges tape-fed to a combustion chamber, is attractive from the standpoint of high specific impulse but is discarded from consideration for Voyager because of low reliability. The mechanization which feeds the solid propellant charges is complex and has demonstrated low reliability during development. The hydrogen-peroxide monopropellant and the water electrolysis systems are eliminated from consideration on the basis of safety. In several systems, hydrogen peroxide has gone unstable resulting in decomposition and storage pressure increases. In the water electrolysis system the products (namely, a stoichiometric mixture of hydrogen and oxygen) are stored in a plenum. The explosive tendencies of this system have inadvertently been demonstrated during developmental tests.

The monopropellant hydrazine system is eliminated from consideration because of the 0.2-pound thrust requirement. Hydrazine engines have been flown with thrust levels down to 0.5 pound, but this is about the current state-of-the-art lower limit for pulse-mode thrusters. Even if a breakthrough is accomplished in the state of the art and thrust levels of 0.2 pound were to become obtainable, the efficiency for pulse mode operation is very low due to the catalyst bed cooling that occurs with extended periods between firing. It is doubtful that specific impulses of 100 lb-sec/lb can be achieved for 0.020-second pulses that occur every

two or three hours in the typical RCS duty cycle; the specific impulse for the hydrazine-plenum system is of that same order and can meet the thrust requirements quite easily.

From the original list, there are basically three remaining systems which can be considered for Voyager which warrant further investigation. The three systems are:

- Cold gas - nitrogen
- Hydrazine - plenum
- Resistance-heated thrusters.

The resistance-heated thrusters use electric energy to heat a metallic resistance element and transfer this heat to the working fluid prior to expansion through the nozzle. The resistance elements could be applied to either the cold-gas nitrogen system or the hydrazine-plenum system. Since the weight advantage for the hydrazine-plenum system would be slight, the resistance heaters will only be considered for the cold-gas nitrogen system. The heated cold gas concept can also be implemented using radio-isotope heated thrusters such as those currently under development at TRW. Although this approach offers significant advantages in weight in as much as electrical power is not required for heating the gas, it has not yet been proven in an actual flight application. Because of lack of operating experience with this system it has not been seriously considered for this analysis.

A discussion of the three types of systems selected for analysis follows.

1. COLD GAS - NITROGEN

Historically, the cold-gas nitrogen system has been used for reaction control systems more than any other system. The gas is stored in high-pressure (3000 to 4000 psi) titanium vessels, pressure regulated to a low pressure (30 to 50 psi), and then distributed to solenoid valves and converging-diverging nozzles. To protect against the failure of any single component, the concept for half systems each carrying 1.5 times the mission gas requirement has evolved and has been used successfully.

For Voyager, the high and low thrust levels would be accomplished by using the same solenoid valves and thrusters and a high- and low-pressure regulator. When high thrust is desired, the high-pressure regulator is switched into the system. For low thrust, the high-pressure regulator is switched out. This approach is more reliable and less complex than a system involving one regulator and high-thrust valves and nozzles and low-thrust valves and nozzles. The calculated total system weight for the cold-gas nitrogen system for a Voyager-type mission is 155 pounds, and the calculated reliability for a half system is 0.9891.

The impulse carried by each half system can be reduced from 1.5 to 1.0 by the use of squib valves and a scheme for failure detection. By inserting a normally open squib valve between the solenoid valves and the regulator, a failed-open solenoid valve in one half system can be detected and the squib valve actuated. Since the remaining half system does not counteract the force of the open thruster, the amount of gas carried in each half system can be reduced to 1.0 times the mission requirement.

The problem of failure detection is a difficult one. Observing the spacecraft limit cycles and the pressure vessel pressures from ground telemetry is probably the most straightforward way to determine if a valve has failed "open" and in which half system it is located. Ground command could then be utilized to activate the appropriate squib valve. The major disadvantage to this approach is that there may be periods of time when the spacecraft is not in communication with earth. A considerable amount of gas may be lost if a solenoid valve sticks open immediately after occultation of Mars and is not discovered until the spacecraft exits the occultation zone and communication is re-established. The alternative is on-board logic which senses pressure decay rates as well as limits cycle data and compares these to preset levels. Exceeding the preset levels results in an automatic closing of a squib valve.

Another approach which results in roughly the same systems weight as for the squib valve system is to place two solenoid valves in series for each thruster. If one valve sticks open, the series valve prevents gas depletion. The advantages to this approach are that no failure detection

is required and the system can return to normal operation if the valve should "unstick"; this would be virtually impossible with a one-shot squib valve system. The major disadvantage with this type of system is that the probability of a particular thruster failing to produce thrust is increased since two valves in series must open. The failure probability can be reduced by using quad-redundant valves with a weight increase.

The calculated reaction control system for the same Voyager-type mission reliability for a half system with the quad-redundant valve configuration is 0.9950, and the total system weight is 136 pounds.

The possibility of reducing the cold-gas nitrogen system weight further is remote within the constraints of this study. Protecting against a leak or meteoritic impact on a pressure vessel, for example, requires two storage vessels and at least 1.0 times the mission-required impulse to be stored in each vessel.

2. HYDRAZINE-PLENUM

The hydrazine- plenum system is basically a cold-gas system with the nitrogen storage tanks replaced by a hydrazine monopropellant gas generator and a plenum chamber. Two half systems would be employed for Voyager, as shown in Figure K-1, the hydrazine is stored in a bladdered tank under relatively low pressure (500 psi). Pressure switches open or close the solenoid valve which controls the flow of liquid hydrazine to the catalyst bed. At the catalyst bed (Shell 405), the hydrazine is

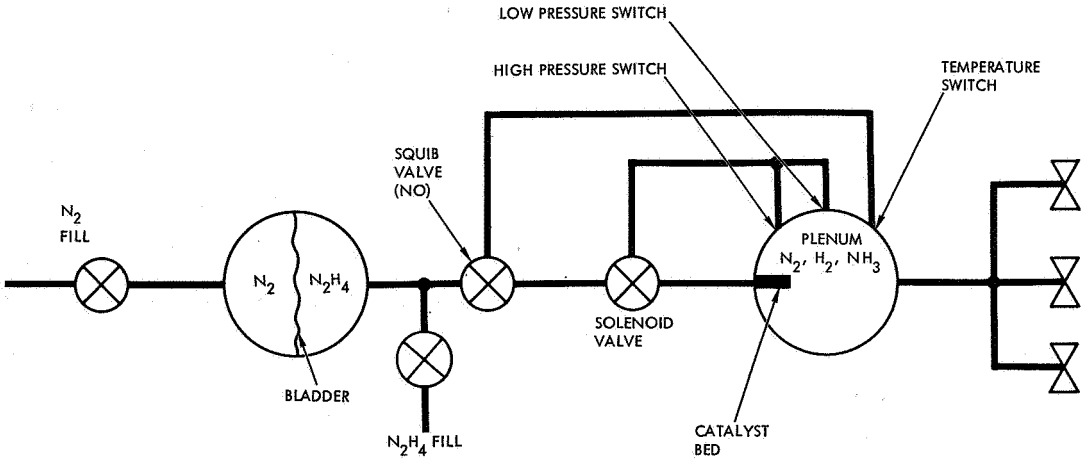


Figure K-1. Hydrazine — Plenum Half System

decomposed into nitrogen, hydrogen, and ammonia in an exothermic reaction. The products of dissociation are trapped in a plenum to be used on demand by the solenoid valves and thrusters. The pressure within the plenum is controlled within the deadband of the pressure switch; high and low thrust levels are obtained by using both a high-pressure switch and a low-pressure switch. With the high-pressure switch the plenum pressure would be approximately 350 psi and the low-pressure switch would regulate the pressure at roughly 23 psi.

Since the gases remain in the plenum chamber for some time before being expelled, the gas temperature would be reduced to near ambient, resulting in a specific impulse of roughly 100 to 115 lb-sec/lb. This, combined with the low-pressure storage, results in a considerable savings in total system weight over the nitrogen-type system.

As stated before, the dissociation of hydrazine is exothermic so that failure mode conditions must be looked at carefully. The technique of using three times the system impulse in two half systems to protect against the valve "open" failure is not applicable to this system. If such a scheme were employed, the open valve would result in the gas generator firing continually to meet the demand, and the heat generated would soon raise the spacecraft temperature to catastrophic levels.

It would appear that the only reasonable approach is to use a squib valve activated by a temperature transducer as shown in Figure R-18. In the event of a valve open failure or a gross plenum leak (meteoritic impact), the hydrazine flows until the temperature reaches a preset level and activates the squib valve. At this point, the flow of hydrazine is stopped and the remaining half system merely must provide the impulse for the remainder of the mission without counteracting the force from the failed valve. Thus, a total of 1.0 times the mission impulse requirement must be carried in each half system to protect against any single component failure. The calculated total system weight for the hydrazine-plenum system is 40 pounds, and the calculated half system reliability for this approach is 0.9466.

Table K-1. Voyager Candidate Reaction Control Systems— The heated Nitrogen System is Preferred because a Significant Weight Advantage is Realizedwith Virtually the same Reliability as the Conventional Nitrogen System at a Higher but Acceptable Power Level

System Approach	Weight (lb)	Peak Power (w)	Reliability per Half System
1. Nitrogen system (three times mission-required impulse)	155	202	0.9891
2. Nitrogen system (two times mission-required impulse quad-redundant valves)	136	652	0.9950
3. Heated nitrogen system (three times mission-required impulse)	143	250	0.9887
4. Hydrazine-plenum system (two times mission-required impulse)	40	230	0.9466

3. RESISTANCE-HEATED NITROGEN

Using a temperature of 1500°F, the resistance-heated nitrogen system recommended for Voyager would provide a nitrogen specific impulse of approximately 120 lb-sec/lb. Since the power required to heat the gas would be too high for high-thrust mode, it is proposed that the heated thrusters be used for only the low-thrust mode.

The calculated total system weight is 143 pounds, and the calculated reliability for a half system is 0.9887.

4. VOYAGER REACTION CONTROL SYSTEM SELECTION

The weights, peak power, and reliability for the variations of the three basic types of systems are summarized in Table K-1. From this

table, it is clear that some systems are unacceptable for Voyager use. The nitrogen system with quad-redundant valves has a very high reliability with a reasonable weight, but the power required is unreasonable. In addition, the packaging problems associated with placing four valves in close proximity to the nozzle become ludicrous when one considers that up to four nozzles may be located in a single cluster, thus requiring 16 solenoid valves in the package. The heated nitrogen system is preferred over the conventional nitrogen system since a significant weight advantage is realized with virtually the same reliability as the conventional nitrogen system but at a higher but acceptable power level.

It would appear, therefore, that the ultimate selection is between the hydrazine-plenum system and the heated nitrogen system. Although both systems are acceptable for Voyager on the basis of weight, power, and reliability, the hydrazine-plenum system offers a significant reduction in weight but at a reduced reliability level.

At this point it is not clear whether the hydrazine system weight offsets the reduction in reliability. There are several points, however, which should be discussed. For one, a hydrazine propulsion system using a catalyst bed has never been used in a spacecraft application. Hydrazine engines flown thus far use N_2O_4 to start the decomposition with only a few restarts designed into the system; this clearly is unacceptable for the Voyager application. The second point to be considered is that some major problems have been uncovered in ground development testing of the hydrazine-plenum system. The Shell 405 catalyst bed is a continual source of particulate contamination in the 1- to 20-micron range which would degrade the solenoid valve reliability almost catastrophically. The alternative is to filter the gas before passing it through the valves. Filtering attempts thus far have proven to be rather futile in that such large quantities of contamination are generated that even large area filters are subject to plugging in relatively short periods of time. Another problem uncovered in developmental tests is the decomposition products of hydrazine. Since the catalyst bed is used only once in a period of hours, the

bed cools and inefficient start-ups occur. This results in raw hydrazine being admitted to the plenum chamber and expelled through the valves. Making the solenoid valves and seals hydrazine-compatible has proven to be rather difficult.

In short, there are several problems inherent with the hydrazine-plenum system that must be solved and demonstrated before the system can be considered for spacecraft use. Since the heated nitrogen system has been successfully flown on several spacecraft and the weight is within acceptable levels and the reliability considerably better, its use on Voyager is recommended.

APPENDIX L

ENGINE ACTUATOR TRADEOFFS

Three alternate thrust vector control actuator systems we considered for application to Voyager: 1) a magnetic particle clutch actuator; 2) a hydraulic blow-down system; and 3) a hydraulic pump system. Table L-1 presents the tradeoff analysis and compares the three systems with the proposed DC torque motor actuator.

The magnetic particle clutch actuator uses counter-rotating clutches driven by DC motors. A command current to the appropriate clutch applies a proportional torque to a ball screw, which converts the torque to a linear force. An advantage of the magnetic particle clutch actuator is its fast response and its resistance to being back-driven while de-energized. A major drawback is the magnetic particle clutch itself. One manufacturer (Cadillac Gage) is extremely skeptical about whether the present Apollo Service Module actuator can be scaled down to Voyager thrust vector control requirements. Evidently, the state of the art for magnetic particle clutches has not advanced to the point where it can safely be considered for this application. Furthermore, there are two modes of failure which can jeopardize the mission: the shifting of the particles, causing dynamic unbalance; and the migration of particles through the seal to the bearings, causing premature wear.

The hydraulic blow-down system uses the energy of stored gas to create hydraulic pressure which moves a piston. The gas is regulated to obtain a steady pressure. Command electric currents operate a servo valve which regulates the flow of hydraulic oil. Another reservoir is needed to collect the expended oil. The chief advantages of this system are low electric power (5 watts) and also low power to hold the actuator in position, only hydraulic power to take care of the leakage. The major disadvantages are: the weight is high because oil must be carried on board to provide for about 18 minutes of operation (the weight of the oil alone is about 33 pounds); and all hydraulic systems are susceptible to external leakage and to other failures, such as oil gumming, drying out of seals, and fluid contamination.

Table L-1. Thrust Vector Control Tradeoffs Show That the Hydraulic Pump System and the DC Torque Motor/Ball Screw Actuators are Most Suitable for the Voyager Spacecraft

System	Performance	Weight (lb) (Two-Axis Control)	Power	Cleanliness	RFI	Life and Reliability	Comments
Magnetic particle clutch	Fast response, large torque	36	800 watts, average; 1400 watts, peak	Magnetic clutches	None	Moderate reliability	Mechanically complex
DC torque motor with ballscrew	Smooth operation	48	260 watts, average; 375 watts, peak	PM fields	Brush noise	High reliability	Easily fabricated, assembled, and tested
Hydraulic pump system	Fast response; excellent holding capability	26	50 watts, average; 150 watts, peak	No PM fields	No RFI generated by motor	Moderate reliability	Needs to be started up a few minutes before use; no prior spacecraft experience
Hydraulic blow-down	Fast response excellent holding capability	70.0	5 watts, control	No magnetic fields	None	High reliability	No prior spacecraft experience

The hydraulic pump system uses an accumulator to supply peak hydraulic power to the actuator. A small pump is used to supply power to provide for internal leakage. This system is the lowest weight system considered. It has fast response and excellent holding capability. It uses less electric power because it does not have to handle peak loads (these are smoothed out by the accumulator). Its chief disadvantages are that it is less reliable since it needs an electric motor plus the other parts of a hydraulic system (accumulator, servo valve, relief valve, filters, etc.) and any hydraulic system has certain modes of failure such as leakage contamination which are difficult to protect against. The use of hydraulic systems for long periods in space is still untried, although long-term storage of hydraulic systems is common practice in missile technology.

From the tradeoff study, it appears that either the DC motor/ball screw actuator or a hydraulic pump system (shown in Figure L-1) are the best choice for the thrust vector control actuators. The weight and power for the hydraulic system are lower but at the expense of reliability. As mentioned before, the hydraulic system is basically untried in a spacecraft application and the reliability level is more of an unknown factor. For this reason, the DC motor/ball screw actuator, which has a significant amount of spacecraft experience, is selected for the thrust vector control actuators. The hydraulic pump system, however, does have some significant advantages; redundancy techniques and special attention to leakage could make this approach preferable.

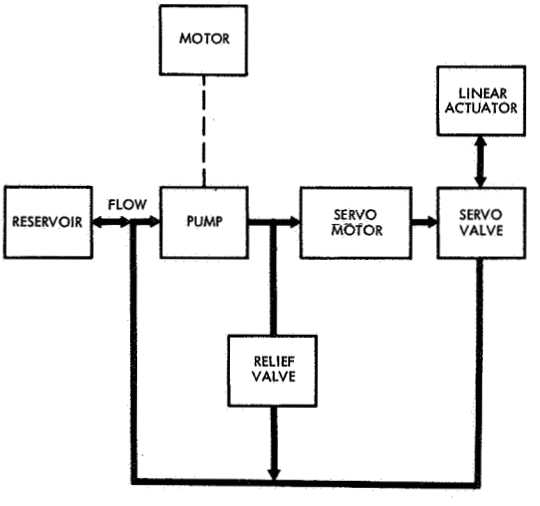


Figure L-1. Hydraulic Pump System

APPENDIX M

DIGITAL CONTROL STUDY

1. INTRODUCTION

This appendix presents the results of an initial study performed to establish a digitized configuration for the Voyager guidance and control subsystem (Section 5). At the outset the decision was made to constrain the study to the digitization of the present Voyager analog guidance and control subsystem.

2. SUMMARY

The digitization of the present analog guidance and control subsystem functions offers several advantages:

- Elimination of external mode switching
- Acquisition without gyro backup
- Reduced acquisition fuel requirement
- Elimination of the drift problem in analog integrators and long-time constant networks.

In the digital guidance and control system the mode switching, loop gain switching, and deadband changes will be implemented by means of internal computer logics.

The performance of the digitized system will be essentially identical to the analog system. However, in the acquisition mode, the digital system uses the optimum deadbeat control law. Thus, the digital system will converge into the desired position without overshoot. In addition, the system will converge without the need for rate gyro or lead-lag augmentation.

In the present analog thrust vector control, analog integrators provide error integration feedback. These analog integrators are extremely sensitive to unsymmetrical electrical noise and null shifts. The digital implementation will eliminate both problems. Essentially the digital thrust vector control loop will be similar to the analog thrust vector control loop with the addition of sensor interface units and the digital compensation networks.

For the digitized system it appears advantageous to change the gyro reference assembly unit into a digital system using pulse torquing, operating the gyro loops in closed-loop. This method will provide direct interface of the gyro unit into the computer.

In the quantization of analog signal into digital data, it is highly desirable to restrict the signal spectrum of the analog device before sampling. The filter characteristic should be low pass with cutoff bandpass set at less than one half the sampling frequency.

3. DIGITIZED GUIDANCE AND CONTROL CONFIGURATION

Functionally the digitized guidance and control configuration will be identical to the present analog guidance and control configuration. The areas of major distinction between the analog guidance and control subsystem and the digitized guidance and control subsystem are in the:

- Derived-rate modulator
- Gain change operation
- Deadband switching operation
- Digital lead-lag compensation
- Digital-to-analog and analog-to-digital interface.

A general block diagram of the digitized guidance and control configuration is given by Figure M-1. In the block diagram the assumption is made that the present computer and sequencer functions will be performed by the computer.

Additionally, it appears desirable to redesign the gyro reference assembly to provide closed loop gyro operation, using pulsed torquing in conjunction with a digital counter to provide concurrent rate and position data. With this method the gyro will be interfaced directly into the computer without an intermediate analog-to-digital converter.

The closed loop gyro operation will permit maneuvering without the use of the precision current generators. Thus, to perform a maneuver, the computer first clears the gyro position counter and directs the gyro counter output into the attitude control loop. The maneuver command may be done in a single step slew or by means of a ramp command (e.g., in

0.2 deg/sec steps until the desired position is reached). A large maneuver is performed by loading the desired angle into the gyro counter and allow the gyro counter to count down to zero.

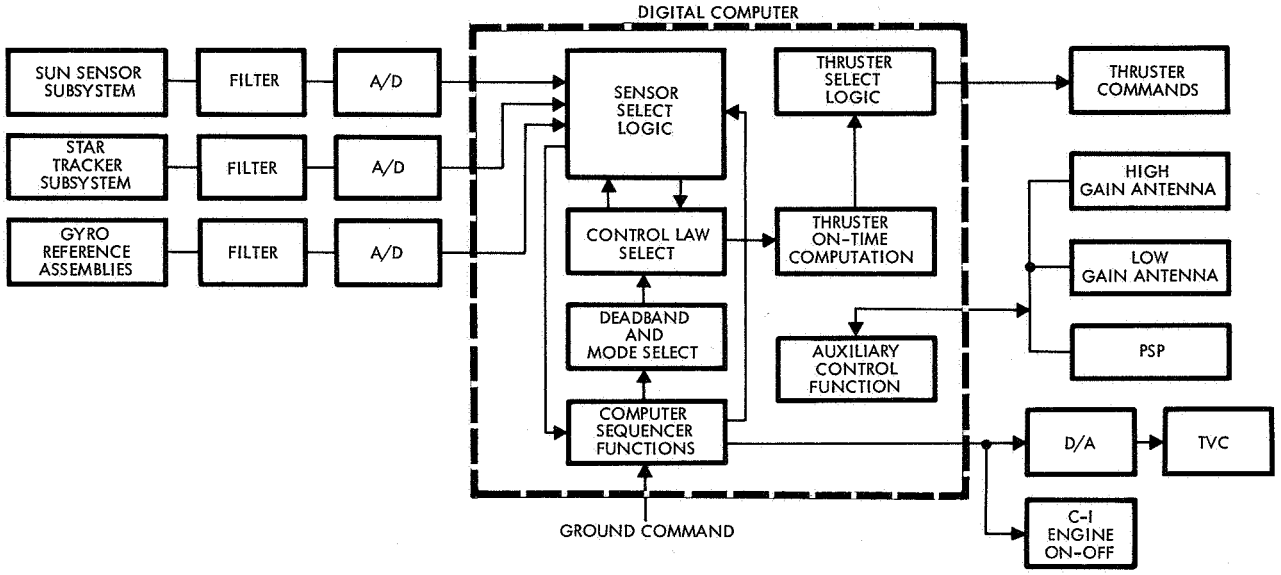


Figure M-1. Digitized Guidance and Control System

3.1 Digital Derived Rate Modulator

Two methods of implementing the derived rate modulator have been considered. The first consists of direct digitization of the modulator using logic to establish the thrust commands. A block diagram of the derived rate modulator is given by Figure M-2. The design parameters for the Voyager attitude control loop indicate the minimum thrust command pulse duration to be 0.025 second. It is desirable to control the thruster pulse duration to within a millisecond. A clock at least 1 kc will be required as input to the up-down derived rate counter. The modulator loop must also operate at a minimum of 1 kc.

The deadband logic diagram is given by Figure M-3. In this implementation the complete logic is cycled each time at a 1 kc rate. In the

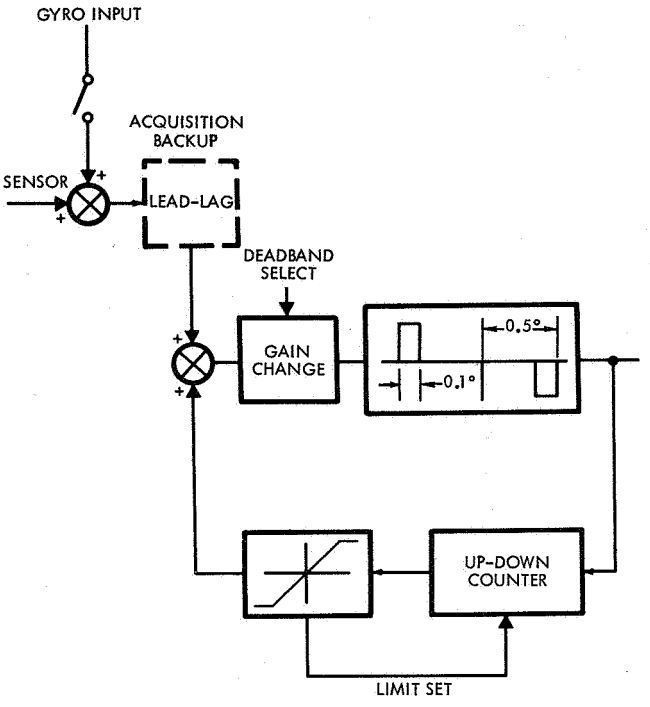


Figure M-2. Derived Rate Modulator

diagram the thruster command gate which has state zero or one is used as a bookkeeping device.

The derived-rate filter is implemented by an up-down counter using a linear approximation of the lowpass rate filter. In the time domain the rate filter output to a step input is given as:

$$C_o(t) = \pm T_o K(1 - e^{-t/\tau})$$

where the input, C_i, is specified as

$$C_i = \text{step} = \pm T_o \text{ (proportional to control torque)}$$

The linear approximation is obtained by series expansion of:

$$e^{-t} = 1 - x + \frac{x^2}{2!} - \frac{x^3}{3!} + \cdots$$

$$C_o(t) = \pm T_o K \frac{t}{\tau}$$

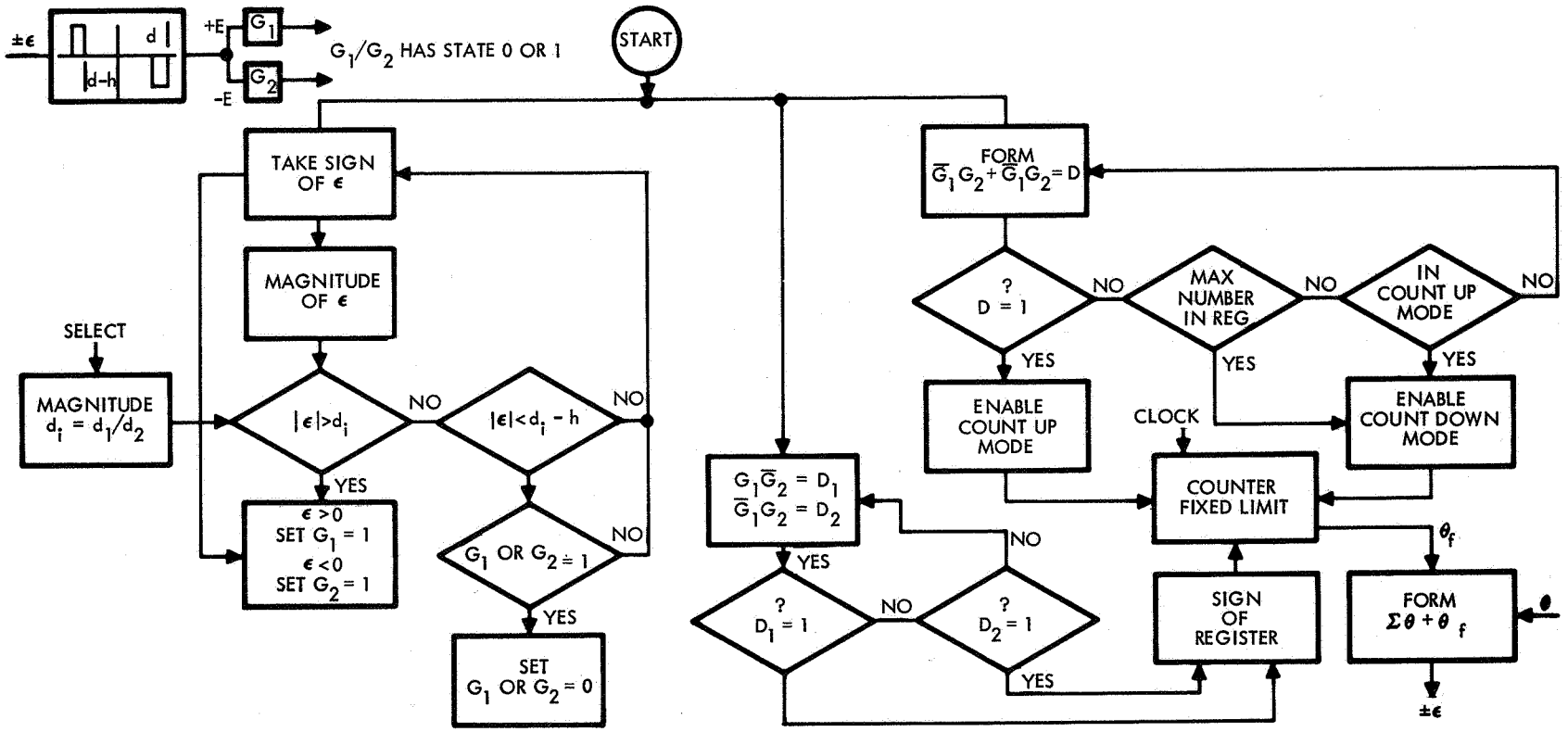


Figure M-3. Deadband Logic Diagram

The up-down counter output is given as:

$$C_t = \sum_{o}^{n} \pm A\delta(t - T_n) - \sum_{o}^{m} \pm A\delta(t - T_m)$$

where A is the granularity of the count steps in degree/count. Also

$$\sum_{o}^{m} A\delta(t - T_m) \leq \sum_{o}^{n} A\delta(t - T_n)$$

n starts at thruster ON command
m starts at thruster OFF command
m/n do not occur simultaneously
T_n, T_m clock rate

The analog derived rate modulator rate filter has a limit which limits the maximum output of the filter. In the digital system this is done by fixing the maximum count of the counter register.

The major disadvantage of this digitized derived rate modulator is that the internal loop computation must be done to the desired thruster on time accuracy. Thus, in order to control the thruster on time to a millisecond accuracy, the computer must operate at a 1 kc solution rate.

An alternative, preferred, implementation of the derived rate modulator is by direct computation of the attitude control impulse by the computer. This modulator has two modes of operation. The small error operation is essentially a derived rate modulator. The large error operation is by means of optimum switching technique.

The computation cycle rate has been selected to be 100 milliseconds. For small rate and error angle operation, the computer computes the thruster command ON time as:

$$t_{ON} = \frac{\theta_i + \theta_h - \theta_d}{\frac{T_o K}{\tau}}$$

where

θ_i = attitude error at sampled instance

θ_h = hysteresis angle

θ_d = semi-deadband angle

Tentatively, the small error and rate boundary has been set as:

$$\theta \leq 5 \text{ deg}$$

$$\theta \leq 0.5 \text{ deg/sec}$$

Using the parameter selected for the present analog configuration, calculate the minimum impulse bit for the digital system.

Analog minimum impulse bit is given as:

$$t = -\tau \, 1_n\left(1 - \frac{\theta_h}{KT_o}\right)$$

where

$\tau = 50$ sec

$\theta_h = 0.1$ deg

$K = 52$ deg/ft-lb

$T_o = 0.2$ lb (19.3 ft) = 3.86 lb-ft

$t = -50\,(-0.1/200) = 0.025$ sec.

The digital minimum impulse bit is given as

$$t = \frac{0.5 + 0.1 - 0.5}{T_o K} \tau = 0.025 \text{ sec}$$

For the arbitrary selected boundary of the 5 degree attitude error and 0.5 deg/sec attitude rate, the control law equation is given by

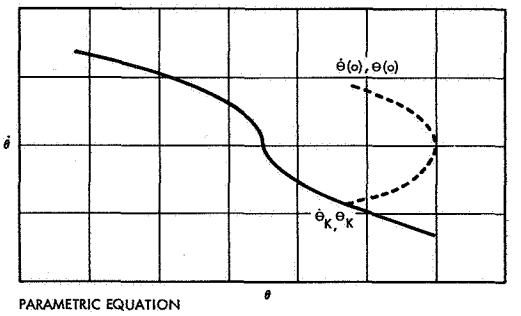
$$t_{ON} = \frac{\theta_i + \theta_h - \theta_d}{\frac{T_o K}{\tau}}$$

This equation has not been analyzed in detail for convergence. However, some rough hand calculation has been made and the results show that it does converge. The operation of this pulsewidth modulator will be identical to the derived rate modulator for small error rates.

The two units are identical when the derived rate filter output at each thruster command is zero.

For large angle operation such as required for reorientation maneuver and initial acquisition, the control law is based upon switching the system at the optimum deadbeat response curve as defined in the phase-plane. The computer initially looks at the spacecraft attitude error as measured by sensors. It also computes an estimate of the error rate. If the spacecraft state vector does not coincide with the optimum switch line state, the computer issues commands to the thruster to reduce the initial rate while converging toward the optimum switching point. The thruster will stay on until it reaches the optimum switch line at which time the initial thruster is turned off and an opposite thruster is turned on for a precomputed duration. The computation is based on the time required to null the initial rate established at the optimum switch line.

A plot of the optimum switch line is given by Figure M-4. The parametric equation is very simple and it is stored in the computer. In actual operation the computer estimates the spacecraft state from sensor or gyro information and tests whether the optimum switch line conditions are satisfied.



PARAMETRIC EQUATION

$\dot{\theta}^2 - 2_c\theta = 0, \quad \lambda_c = \frac{T\ell m}{I}$

THRUSTER ON-TIME TO NULL

$t_{ON} = \frac{\dot{\theta}_K}{\lambda_c} = \frac{2\theta_K}{\lambda_c}$

$\dot{\theta}_K, \theta_K$ CORRESPONDS TO VEHICLE STATE AT THE OPTIMUM SWITCH LINE

Figure M-4. Optimum Switch Line

The advantage of this approach is threefold: 1) this method enables the computer to operate at a relatively slow computation cycle rate of 10 samples per second or less, 2) acquisition time will be shorter, and 3) propellant utilization for acquisition will be less.

3.2 DIGITAL FILTER

The implementation of filter transfer functions by means of digital computer is simple and straightforward. The simplest approach is to obtain the z-transform of the filter transfer function. Using the z-transform approach, the exponents of z denote the staleness of the input in terms of the sample period. The coefficient associated with each z^{-k} term is the value of the function of the kth sampled time.

In the present Phase 1A, Task B, guidance and control design plan, lead-lag filter may be used as acquisition backup for the attitude control loops. Under the digital attitude control loop design presented in this report, neither lead-lag filter nor gyro are required for acquisition. However, digital compensation network will be required in the thrust vector control loops. The discussion in the section will be directed toward digital implementation of a general transfer function.

Any transfer function may be converted into a z plane function by table look up in numerous sampled data textbooks. However, it may be easily computed by

$$G(z) = \sum_{k} \text{residues of } \frac{G(\alpha)}{1 - e^{T\alpha} z^{-1}}$$

where

α is a pole at S_k

T is the sampling period

In general, any transfer function may be represented as

$$G(z) = \frac{E_o(z)}{E_1(z)} = \frac{a_o + a_1 z^{-1} + a_2 z^{-2} + a_3 z^{-3} + \cdots a_n z^{-n}}{1 + b_1 z^{-1} + b_2 z^{-2} + b_3 z^{-3} + \cdots b_n z^{-n}}$$

$$= \frac{\sum_{o}^{n} a_k z^{-k}}{1 + \sum_{o}^{n} b_k z^{-k}}$$

From a signal flow viewpoint the computer implementation of the G(z) is shown by Figure M-5. As shown in Figure M-5, each z^{-1} represents a storage of one sampling period. The transfer function coefficients are weighing factors for the respective signal lines.

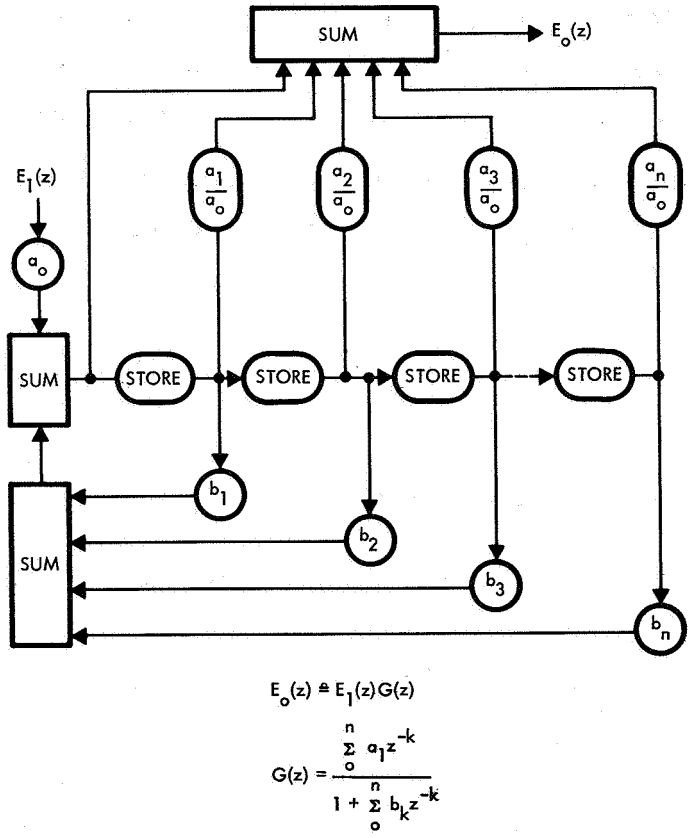


Figure M-5. Implementation of the Digital Transfer Function

Since the input signal to the computer is in the time domain, it appears more reasonable to express the computation mode in time sequence. Since

$$\frac{E_o(z)}{E_1(z)} = \frac{\sum_{o}^{n} a_k z^{-k}}{1 + \sum_{o}^{n} b_k z^{-k}}$$

and

$$e^*(t) = z^{-1}\left[E(z)\right]$$

take the cross product of $E_o(z)/E_1(z)$ and perform an inverse z-transform operation gives the difference equation as

$$e_o^*(t) = \sum_{k=0}^{n} a_k e_i^*(t - kT) - \sum_{k=1}^{n} b_k e_o^*(t - kT)$$

where

$e_i^*(t - kT)$ input at the kth sampling time

$e_o^*(t - kT)$ output at the kth sampling time

For example given the lead-lag network transfer function as

$$\frac{E_o(z)}{E_i(z)} = K \frac{1 + a_1 z^{-1}}{1 + b_1 z^{-1}} \qquad a_1 > b_1$$

$$E_o(z) + b_1 E_o(z) z^{-1} = KE_i(z) + KE_i(z)\, a_1 z^{-1}$$

$$E_o(z) = KE_i(z) + KE_i(z) a_1 z^{-1} - E_o(z)\, b_1 z^{-1}$$

$$e_o^*(t) = Ke_i^*(t) + Ka_1 e_i^*(t - T) - b_1 e_o^*(t - T)$$

The computer requirement for this simple lead-lag network consists of forming four products, performing three sums and the storing of two past values.

3.3 Sampling Operation (A/D Conversion)

In the digitized guidance and control system all of the sensor subsystems must be sampled. In the sampling of an analog signal a few simple rules must be observed. The sampling theorem stated that if a signal f(t) has a spectrum of f_o, the sampling period (T) must be $T = 1/2f_o$.

The mean square quantization error is given as

$$\overline{E}^2 = \frac{q^2}{12}$$

where q is the sampler bit size or resolution of the encoding process.

The major problem area in the sampling operation is in the translation of high frequency noise into the low frequency signal band. The major significance of this is that unless the analog signal has a filter which restricts the output noise spectrum, the sampling operation will increase the noise content of the desired signal.

The proof of the previous statement is found in the examination of the sampling process.

Let $e^*(t) = p(t)\, e(t)$ where $e^*(t)$ denotes the sampler output, p(t) denotes the sampling modulator with fixed period and finite dwell time p. Since p(t) is a periodic function it may be expanded into a Fourier series as

$$p(t) = \sum_{-\infty}^{\infty} A_n e^{jn\omega_s t}$$

where $\omega_s = 2\pi/T$ the sampling frequency. The Fourier series coefficient is given as

$$A_n = \frac{1}{T} \int_o^T p(t) e^{-jn\omega_s t} dt$$

Let $|p(t)| = 1$ and since $0 < t < p$

$$A_n = \frac{1}{T} \int_o^p e^{-jn\omega_s t} = 1 - \frac{e^{-jn\omega_s p}}{j\omega_s T}$$

or simply by trigonometric identities

$$A_n = \frac{p}{T} \frac{\sin \theta}{\theta} e^{-j\theta}$$

where

$$\theta = n\omega_s p/2$$

therefore

$$e^*(t) = \sum_{-\infty}^{\infty} \frac{p}{T} \frac{\sin \theta}{\theta} e^{-j\theta} e(t) e^{jn\omega_s t}$$

Since e(t) is a continuous time function it may be converted into the frequency domain by means of the Fourier transform.

$$F\ e^{jn\omega_s t} e(t) = E(j\omega - j\omega_s)$$

therefore

$$E^*(j\omega) = \sum_{-\infty}^{\infty} \frac{p}{T} \frac{\sin \theta}{\theta} e^{j\theta} E(j\omega - jn\omega_s)$$

The magnitude of $E^*(j\omega)$ is given as

$$|E^*(j\omega)| = \sum_{-\infty}^{\infty} \left| \frac{p}{T} \frac{\sin \theta}{\theta} E(j\omega - jn\omega_s) \right|$$

Take the ideal case where the dwell time p approaches zero since

$$\lim_{p \to 0} \frac{\sin \theta(p)}{\theta(p)} = 1$$

The $E^*(j\omega)$ magnitude is given as

$$|E^*(j\omega)| = \sum_{-\infty}^{\infty} |E(j\omega - jn\omega_s)|$$

Assume that $E(j\omega)$ has the following frequency spectrum and examine the spectrum plot about $n = 0$ and $\omega > \omega_{s/2}$

The input frequency spectrum with respect to the sampling frequency is given by Figure M-6. The sampler output spectrum is given by Figure M-7.

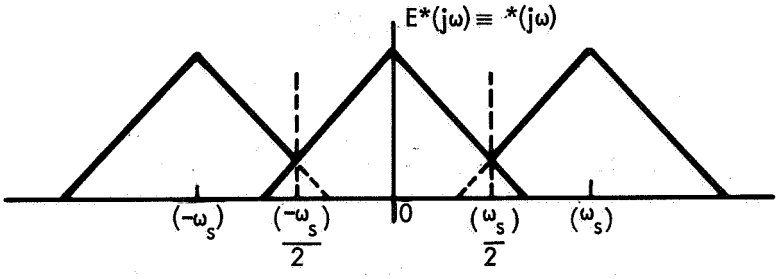


Figure M-6. Input Frequency Spectrum

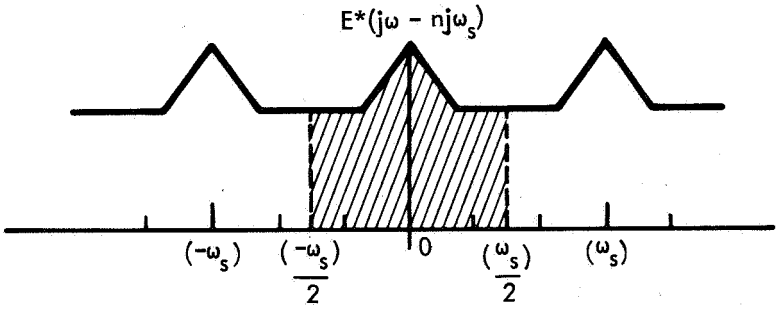
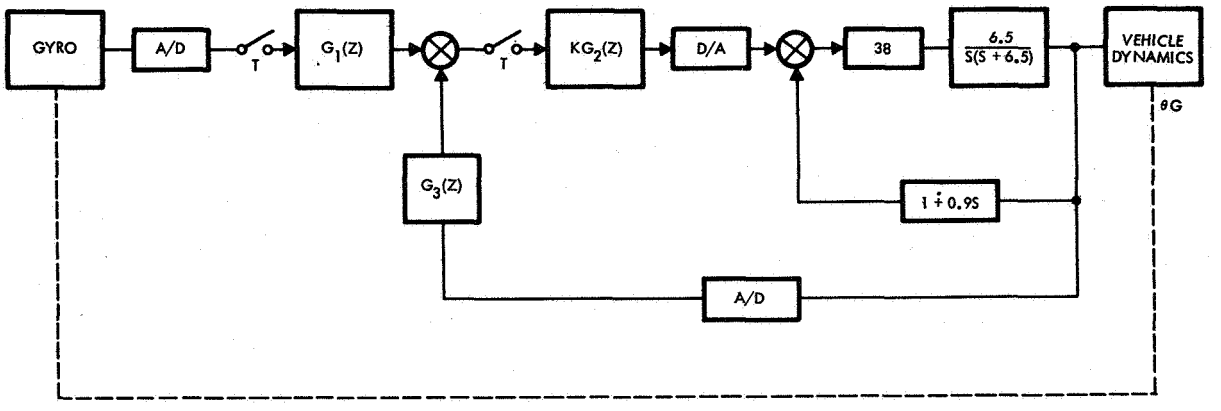


Figure M-7. Output Spectrum

Thus, assuming that the input spectrum greater than $\omega_s/2$ contains mostly undesirable signal, the sampling process increases the unwanted signal content in the desired signal band.

3.4 The Thrust Vector Control Operation

A preliminary block diagram of the digitized thrust vector control loop is given in Figure M-8. The major difference between this and the analog system is the addition of an analog-to-digital converter following the gyro and the addition of a digital-to-analog converter ahead of the input to the actuator control loop. In the digital thrust vector control loop the various compensation networks and feedback integrators are implemented by digital technique.



A/D ANALOG TO DIGITAL CONVERTER
D/A DIGITAL TO ANALOG CONVERTER

Figure M-8. Thrust Vector Control Loop

A detailed study on the analog thrust vector control loop is contained in Section 3.0 of Volume IV of a report entitled "Voyager Support Study, Report No. 04480-6087-R000, July 1967.

The digital sampling for the thrust vector control has been tentatively chosen at 10 samples per second. If the sampling rate is selected such that the system dynamics are slow when compared to the sampling frequency, the digitized system will perform very nearly as the analog system. The major undesirable effects will be the reduction in phase margin and the possibility of high frequency ripple occurring at a multiple of the sampling frequency.

In general the reduction in phase margin for a zero order type data reconstruction is given by

$$\phi = -180 \frac{\omega}{\omega_s}$$

Fortunately, the spacecraft dynamics does not have an equivalent bandwidth to the actuator loop. Using the spacecraft parameters for the start MOI (Mars Orbit Insertion), the spacecraft response to a step thrust vector offset angle is given by Figure 115 of Volume IV of the Voyager

study. Taking the slope of the vehicle attitude response curve, the maximum dynamic response is approximately

$$\frac{0.2 \text{ deg}}{0.4 \text{ sec}} = 0.5 \text{ deg/sec}$$

Therefore $\omega \cong 0.01$.

The reduction in phase margin for the total thrust vector control loop is given as:

$$\phi = -180 \frac{0.01}{62.8} \cong 0.03 \text{ deg}$$

The phase margin given by the analog thrust vector control study shows a minimum phase margin of 40 degrees for all thrust vector control modes. It appears that 10 samples per second will be entirely adequate for the digital thrust vector control loop.

The operating frequency at the start of the Mars orbit insertion phase is 3.7 rad/sec. The reduction in the rigid body phase margin would approximately be:

$$\phi = -180 \left(\frac{3.7}{62.8}\right) = 10.6 \text{ degrees}$$

The rigid body phase margin would be reduced from 38 degrees to 27 degrees, which is still acceptable; however, an increase of the digital lead compensation to increase stability margins would still be desirable. The 10 samples per second rate is considered satisfactory for the digital thrust vector control loop.

3.5 Sensor Interface Requirements

The present guidance and control configuration consists entirely of analog sensors. Under the present digital guidance and control implementation constraints, no changes will be made to the sensor subsystems.

Digital-to-analog conversion devices will be required for all the sensors. The quantization requirement for the sensors is given below.

Sensor Type	Range (deg)	Resolution (deg)	Digital Quantization	Quantization Error σ^2
Coarse sun sensor	±180	±0.7	1 bit sign 8 bit angle	0.04 deg^2
Fine sun sensor	±10	±0.04	1 bit sign 8 bit angle	1.3×10^{-3} deg^2
Canopus tracker				
roll	±2.0	±0.03	1 bit sign 6 bit angle	
pitch	±15	±0.08	1 bit sign 8 bit angle	5.3×10^{-4} deg^2
Gyro position	±15	±0.03	1 bit sign 9 bit angle	7.5×10^{-5} deg^2

3.6 Simulation Requirement

It should be noted that computation round off error may cause undesirable parameter shifts in the digital networks. These shifts may or may not cause undue changes in the response of the control loop depending upon the sensitivity of the loop to system root parameter changes. In any event, detailed bit-by-bit digital simulation is desirable to check out the design and also to confirm compatibility of the software.

APPENDIX N

CENTRALIZED COMPUTER STUDY

1. SUMMARY

This is an initial study of the feasibility of carrying out all control and computing in the Voyager spacecraft by means of a central general-purpose computer. As a point of departure, the use of a central general-purpose computer to perform all of the controlling and computing functions of the present computer and sequencer subsystem was examined. This was found to reduce the amount of memory used for discrete commands (as a result of the decision capability of the programmed computer) and to provide a system that was easily modified for later upgraded missions simply by programming changes.

The study did not examine use of the computer for data compression, fault isolation, complete centralization of all special-purpose logic, optimized digital control, or approach guidance. However, these are areas in which a central computer promises considerable advantage, to provide increased capability, greater flexibility (within a mission and from mission-to-mission), and economies in hardware. The additional capacity to handle these functions is easily provided in a central computer of modest size.

In the Voyager configuration examined in this study, the computing and sequencing subsystem provides the event timing and sequencing of all the spacecraft functions and the on-board scientific experiments. The computing and sequencing subsystem is fundamentally a special-purpose sequencer which scans its memory every 1-second cycle to issue commands or data to the appropriate subsystem when the sequence identification tag and time relative to that sequence are coincident with sequence counter time. In addition, an accelerometer counter to control the duration of engine burn and a function generator to point the high gain antenna and the planetary scan platform are included in the computing and sequencing subsystem. A detailed description of the subsystem is contained in Section 5 of this appendix.

The study shows that not only is it feasible for the general-purpose computer to perform all timing and sequencing tasks for the spacecraft and scientific experiments, but also it can perform all the computation and timing for all the control loops in the guidance and control subsystem. Discrete commands which are time referenced within a sequence of events can be programmed into routines by use of indexing and a time differential for successive discretes. Singular discrete commands which do not fit into any particular sequence can be handled in a routine which is time differential dependent. The amount of memory utilized for discrete commands can be decreased as a result of the decision making capabilities of a programmed computer.

Control loop equations which are presently handled in an analog fashion within the guidance and control subsystem are directly adaptable to solution by a central computer. Routines can be developed within the computer program such that the digital solution to certain control loop equations can be calculated repetitively within a major program cycle. Examination of the present guidance and control subsystem requirements indicates that a 13-bit computer word will meet the accuracy requirements. The selected 18-bit word computer provides ample flexibility to meet additional accuracy requirements. Present information indicates that the two-axis thrust vector control loop and the three-axis attitude control loop require solution every 100 milliseconds. The remaining five control loops can be solved every second. Accordingly, a 1-second program major cycle with a 100-millisecond minor cycle has been selected. Changes to these requirements can be accommodated. In addition, solution of the control loop equations by a digital computer can accommodate certain modifications by changing the computer program and/or constants which might result in a hardware modification in an analog configuration. Programming, testing, and verification in program changes can be accomplished with ease as compared with hardware changes. The problem of hardware changes necessitating development effort enhances the alternative of the program change approach when applicable.

At present it appears that less than 25 percent of the computer time will be utilized for the above tasks. This provides for ample growth in either the above functions or additional servicing of other spacecraft subsystems which may impose computational requirements at a future date.

Any portion of the computation cycle which is not needed for the flight program may be used for computer self-testing and status checking of other subsystems. Computer programming options would allow for flexibility for additional requirements as they become known.

This report consists of eight sections. A summary of the requirements and constraints is given in Section 2. A general description of the computer subsystem is included in Section 3. The implementation of the various subsystem functions within the computer is detailed in Section 4. A design description of the computer subsystem is given in Section 5. The system reconfiguration and fail-safe considerations are discussed in Section 6. The system reliability estimate is given in Section 7. Finally, the potential capability of a general-purpose computer to perform additional tasks is briefly discussed in Section 8.

2. REQUIREMENTS AND CONSTRAINTS

The computer will perform all the timing, sequencing, and computing tasks which are to be performed by the computer and sequencer subsystem as outlined in Section 5 of the main report. This includes mode of operation switching, event timing for the mission, for a maneuver, or for an orbit. The computer will provide timing and sequencing information to various subsystems including the science subsystem. The computer will accept inputs from the command subsystem, the guidance and control subsystem, and other subsystems and will provide outputs to various subsystems.

The digital computer is required to provide both timed discrete and serial data for control of the spacecraft during the various mission phases. It will perform all the calculations for the three reaction control loops, two thrust vector control loops, two PSP control loops, two high-gain antenna control loops and one low-gain antenna control loop. The computer will provide the necessary operational program and storage so that under nominal conditions, it is capable of executing all functions, specified in Section 5, from launch to the end of the mission. If necessary, a number of midcourse trajectory corrections or Mars orbit trim can be initiated by a ground command.

It will be possible to modify the computer program by ground commands via the command subsystem. The memory contents may be read out over the telemetry link to the ground by another ground command. The computer will provide redundant counters for accumulation of accelerometer outputs and provide time referenced backup for thrust termination. The computer subsystem will be adapted and integrated into the present Voyager baseline configuration without major changes except for the guidance and control subsystem; will provide the necessary program and storage for on-line confidence test and diagnosis of the computer subsystem; and will provide necessary redundancy so that it will achieve suitable reliability under the constraints of weight and power consumption.

The information stored in the computer memory will be nonvolatile in the event of power transient or power dropout.

While the use of digital computers for data compression, filtering, and prediction seems promising, it is assumed that these advanced requirements are out of the scope of the present study. However, a list of possible future applications will be briefly discussed.

3. GENERAL DESCRIPTION

The computer subsystem consists of a digital computer, a timing unit, and a monitor and control unit. The computer is composed of four units: the central processing unit, the memory unit, the input/output unit, and the power regulator. The input/output unit includes the command input module, the output command decoder, the accelerometer counter, and the telemetry register. The central processing unit consists of the arithmetic unit and the central control of the computer. The timing unit provides all the timing signals for the logic and the memory. The monitor and control unit includes a comparator, a shift register, and some logic for generating control signals and timekeeping required for various tests.

To achieve high reliability, a redundant computer is included. This redundant computer can be connected in parallel during maneuver or switched off-line during cruise. In addition, triple modular redundancy has been considered for the timing unit and the monitor and control unit.

3.1 Computer Characteristics

Three different computer designs have been considered for the Voyager application. First, the possibility of using the existing LM Abort Electronic Assembly (AEA) computer has been examined. This approach has the advantage of proven design and adaptable input/output units. The block diagram of this computer is given in Figure N-1. Then a modification of this computer in which arithmetic operations are executed in serial has been evaluated. This design affords low-cost and low-power consumption. The computer block diagram is similar to that in Figure N-1.

Finally, a study has been made of a design in which arithmetic registers and control counters are stored in memory, and retrieved and restored as necessary to execute a given instruction. This design is relatively simple and low cost, yet quite fast and versatile. The block diagram of this computer is shown in Figure N-2.

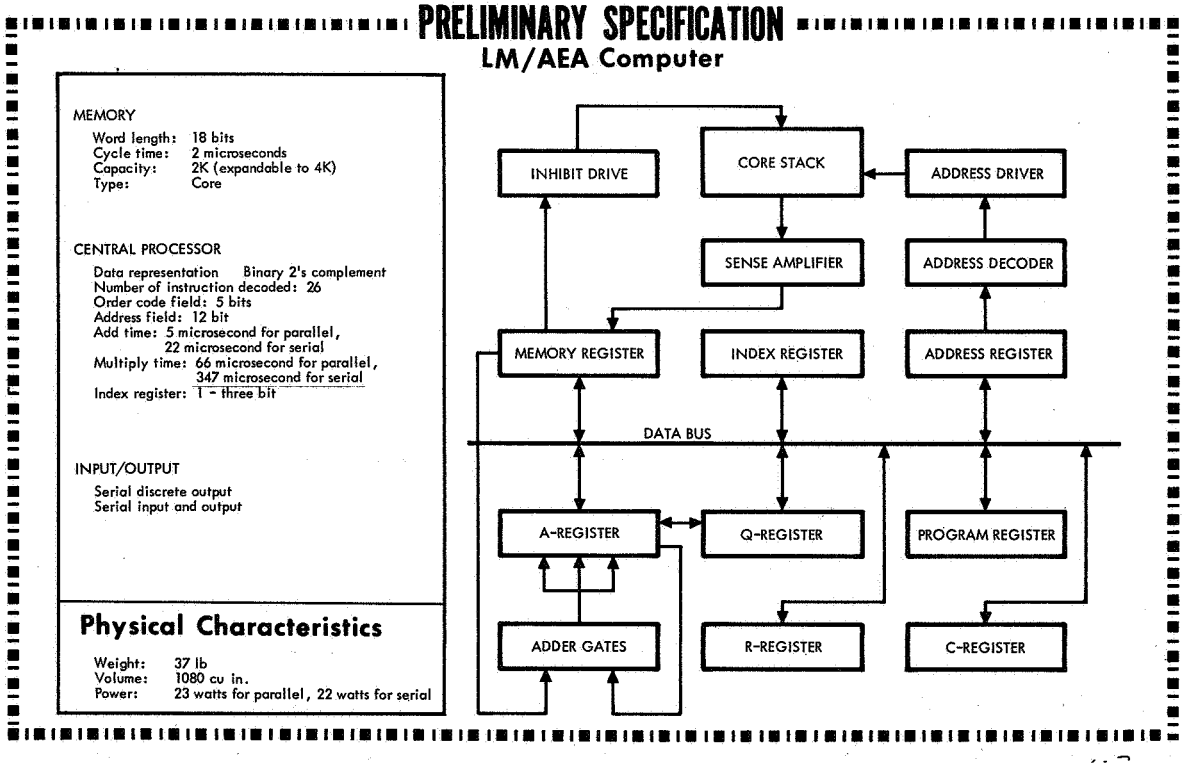


Figure N-1.

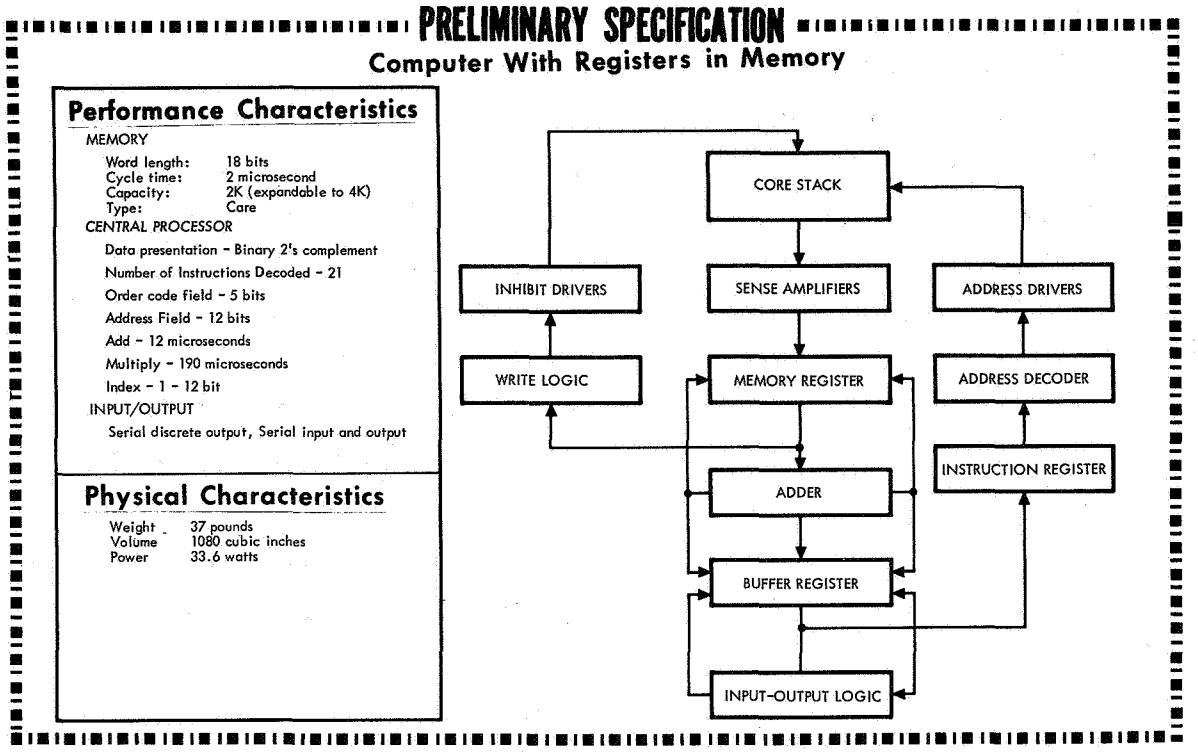


Figure N-2.

Each of these machines is designed around an 18-bit word. The largest word required for computation seems to be 13 bits, but a single address instruction capable of selecting one of 4096 words must have 12 bits for address alone. If five bits are used for the instruction code, and one bit for index control, the total becomes 18 bits. Although the data words might be shorter than instruction words, they are less than one-fourth of the total words required, so it would not be practical to have a separate memory for data.

Since the baseline computer and sequencer subsystem has provisions for issuing up to 512 discretes, the computer must be similarly equipped. This requires 512 instructions, and 512 additional words to establish the times at which these discretes should be issued. There are also time counters, programs to manipulate them, and comparisons with other data. The computer must also process altitude data, and control jets. Thus, the computer should have about 2048 words of storage. To allow for growth, the directly addressable memory can be expanded to 4096 words.

The computer and sequencer subsystem study has a discrete command word that includes an enable (disable) bit which must be set (reset) in order to transmit (inhibit) the command. The digital computer subsystem does not utilize a bit to accomplish this function. If an individual command is to be disabled, the output discrete command can be changed to a no-operation command via the ground link. This is comparable to the computer and sequencer receiving a ground command to disable the command. For a sequence of commands which may all have to be disabled, a single program instruction may be altered by ground command such that the program branches around these commands and they are not executed. The present computer and sequencer requires each command of the sequence to be disabled individually. In both the computer and sequencer approach or the general-purpose computer approach, all changes in memory may be validated via the telemetry.

The memory cycle time for the proposed machine is 2 microseconds. This choice was motivated by the fact that a 2-microsecond memory qualified for aerospace applications is being produced by TRW Systems.

Typical instruction times in microseconds for the three machines, based on a 2-microsecond memory, are:

	LM/AEA	Serialized LM	Parallel Computer with Registers in Memory
Add	5	22	12
Multiply	64	191	190
Divide	66	347	196
Jump	4	4	6

3.2 Physical Characteristics

3.2.1 Power

The power required by the three nonredundant machines without the input/output unit and without the power regulator loss are:

	LM/AEA (watts)	Serialized LM (watts)	Registers in Memory (watts)
Logic	2.8	2.2	1.9
Memory	5.25	5.25	11.4
Total	8.0	7.45	13.3

From experience with the LM/AEA power supply, about 53 percent efficiency may be expected, so total power required will in each case be almost twice that given above. The LM power supply occupies about 300 cubic inches and weighs 11.6 pounds.

3.2.2 Weight and Volume

Most of the space and weight required for these computers would be in the memory; therefore, the figures are the same for all three machine designs.

The input/output system for each machine would require an additional 3.50 watts, and would occupy about 230 cubic inches.

Totals for the three machines are thus:

Machine	LM/AEA	Serialized LM	Registers in Memory
Power	23 watts	22 watts	33.6 watts
Weight	37 lb	37 lb	37 lb
Volume	1080 $in.^3$	1080 $in.^3$	1080 $in.^3$

3.3 Computer Capability

The possibilities for effective use of computer flexibility are sharply limited by the constraints of the baseline system. We can, however, offer some advantage in these cases:

- Multiple counters
- More sophisticated antenna pointing
- Simplification of attitude control system
- Digitized servo systems for antennas and planetary scan platform
- On-board diagnosis and reconfiguration.

Under the constraint that the computer subsystem must be adaptable to the present baseline configuration without major redesign of other subsystems, it is difficult to justify the use of a computer. However, if the subsystems are still in the process of design, we could get full advantage of a digital computer by suitable modification of subsystem specifications. Possible applications of digital computers to enhance system performance are discussed in Section 8 of this appendix.

4. IMPLEMENTATION

4.1 Computer and Sequencer Subsystem

The computer subsystem provides several timers and counters which are used in the present computer and sequencer subsystem:

- Mission Timer – In the computer and sequencer subsystem, the mission timer consists of 26 bits with 1-second granularity giving a range exceeding two years. However, memory comparison is provided only with respect to the 14 most significant bits which yield a granularity of approximately 1.1 hours. Using a programmable computer, two words in memory can be updated to hold up to 17 positive data bits each. This scheme can provide selectable combinations of greater range, finer granularity or variable granularity for either the most or least significant portion of time.

- Maneuver Timer – The computer and sequencer maneuver timer uses 14 bits with 1-second granularity. Utilizing a digital computer word, 17 bits are available to provide greater range and finer granularity.

- Orbit Timer – Presently 14 bits with 4-second granularity. Again, greater range and finer granularity is available with a 17-bit data word.

- Science Timer – The science timer will be comparable to the maneuver timer.

- Command Events Counter – The command events counter will count the number of stored commands issued by the computer subsystem to the other spacecraft subsystems. Via the telemetry subsystem, the ground can keep informed of the total number of commands issued during any period as determined by the contents of the counter at the times the telemetry interrogates the computer.

The above timers and the counter are located in the memory.

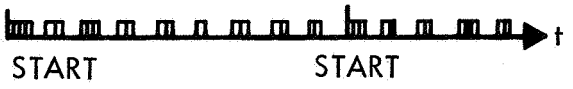
- Function Generator – The function generator of the present computing and sequencing subsystem uses linear approximation to point the high-gain antenna. The fixed change of the command angle for a predetermined time increment is an open-loop process. The present scheme or a refined scheme using a nonlinear approximation can easily be implemented with a digital computer program. In addition, should the requirement arise to close the antenna pointing loop

with the digital computer, a higher degree of accuracy for positioning of the antenna can be achieved.

- Accelerometer Pulse Counter – The velocity correction for the vehicle ranges from 3.28 to 6250 ft/sec with a maximum acceleration of approximately 75 ft/sec^2. The quantization is 0.015 ft/sec pulse yielding a pulse count range of 219 to 417,000 and a maximum pulse rate of approximately 5000 pulses/sec. To retain the scale factor of the accelerometer, a 19-bit counter is required. The accelerometer controls the duration of the engine burn time by issuing a signal after the predetermined number of accelerometer pulses have been counted. By setting the counter initially to the complement of the number of pulses corresponding to the correct ΔV, the overflow of the counter will issue the pulse to terminate the engine burn. The least significant 18 bits of the accelerometer counter are set by an output data instruction, and the most significant bit is simultaneously set to a 1. If it is necessary that the most significant bit be zero, it may be reset by an output discrete instruction. Δ

In addition, the computer subsystem will perform all the timing and sequencing functions which are to be performed by the computer and sequencer subsystem as listed in Section 5 of the Task D Report. The computer program should be capable of utilizing its decision-making features to allow choices of performing or not performing certain commands or sequences. Those commands or sequences which may be repetitions are also conveniently handled by computer programs.

The computer program will have a major cycle time of 1 second and a minor cycle time of 100 milliseconds. A precision 10-cps pulse from the power supply subsystem will be used to define the start of the minor cycle. Every tenth 10-cps pulse will return the program to the start point.



During the 100-milliseconds, the guidance and control loop equations which require solution at a rate of 10 times per second will be solved. The appropriate subroutine will be entered from the program at 10 equally spaced intervals to satisfy this requirement and then return to the

appropriate address in the program. The remaining equations, service routines, diagnostics, etc. will be spaced in the remaining portions of the 100-millisecond intervals in such a manner that the total time for calculations does not exceed 50 milliseconds. The remaining 50 milliseconds are allotted to issue any discrete that may have to be activated during this cycle to other systems. This scheme allows for a maximum of 10 discretes to be issued per second.

4.2 Guidance and Control Subsystem

In the Voyager baseline configuration, all guidance and control functions are performed by means of analog circuits. Functionally, a digitized guidance and control subsystem would remain the same as the analog guidance and control subsystem. However, in the digitized system, the implementation of some of the control laws and components would be by a computer program. The computer program implementation of the various control loops is briefly discussed below. A functional block diagram is given in Figure N-3.

In the attitude control loops, the implementation of the derived rate modulator is by direct computation of the attitude control impulse by the computer. In the small attitude error correction operation, the computer will calculate the time and duration of the thruster-on command. The computer program will have a major cycle time of 1 second and a minor cycle of 100 milliseconds. The computation will repeat every minor cycle. For large angle operation, as in initial acquisition and reorientation maneuvers, the control law is based on switching the system according to an optimum response curve in the phase-plane. The computer samples the spacecraft attitude error and computes an estimated error rate. The computer issues commands to correct the error rate by activating appropriate thrusters and will check the error and error rate against the optimum response curve. The computer will turn off the thrusters when the spacecraft state vector reaches the optimum response curve. Then the computer will turn on an opposite pair of thrusters and will compute the duration required to null the attitude error and the attitude error rate along the optimum response curve. When the attitude error and attitude error rate are reduced below the set values, the computer switches the guidance and control subsystem into the small error correction operation.

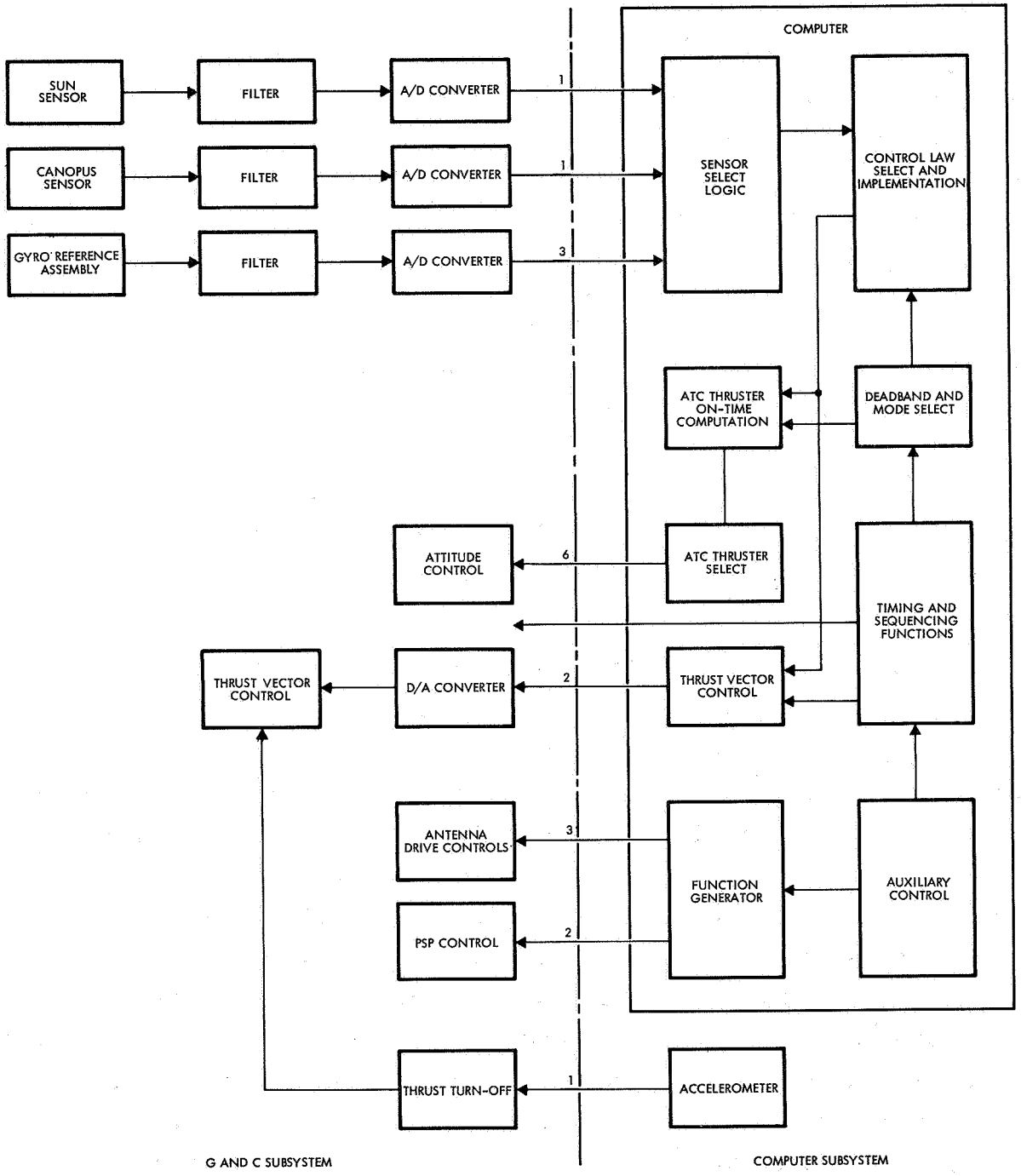


Figure N-3. Digital Computer Implementation of Guidance and Control Subsystems

In the digital thrust vector control loop, the various compensation networks and feedback integrators will be implemented by digital techniques in the computer program. An analog to digital converter following the gyro and a digital to analog converter preceding the input are required in each of the two thrust vector control loops. The computer will sample the data and perform the TVC computation in each minor cycle.

The control of the antenna drives will remain functionally the same as in the present configuration, except the function generator in the computer and sequencer subsystem will be implemented by a computer program. The implementation of the function generator is described in the previous subsection.

The control of the planetary scan platform in the present configuration has a digital interface with the computer and sequencer subsystem. This interface can be directly adapted by the computer subsystem. The computer will compute the necessary angular displacements for the two axes and will provide the appropriate value for the input register of the PSP drive electronic assembly. The computer will also provide necessary control for mode selection.

The control of the antenna drives and the planetary scan platform will be initiated once every major cycle by the computer.

4.3 Command Subsystem

The command subsystem consists of two major units: the demodulator and bit synchronizer, and the command subsystem decoder. The first unit performs the necessary demodulation and bit synchronization for an incoming message from communications subsystem and provides synchronization indication and acquisition control. The above functions are also required to be performed for a digital computer.

Using the Voyager baseline configuration, the command subsystem decoder receives data bits, bit synchronization pulses and decoder lock signals from the bit synchronizer. The decoder contains two channels in a cross-strapped configuration. Each channel consists of an input decoder and an output decoder. The input decoder checks the format and the parity of the incoming messages. It transmits command words either to the output decoder or to other systems. The output decoder provides

discrete commands directly to other systems, including the computer and sequencer subsystem. The command decoder is required to process and transmit commands independent of the computer and sequencer subsystem. This capability enables the ground to control some of the spacecraft subsystems when the computer and sequencer subsystem is inoperative (see Figure N-4).

In the general-purpose computer approach, the format and parity checking could be done by program in the computer. The saving gained by performing this function by the general-purpose computer, however, is outweighed by the loss of direct ground communication with the other subsystem in the event that the computer subsystem becomes inoperative. It is recommended that the functions which are performed by the command decoder be separated from the computer subsystem.

4.4 Telemetry Subsystem

The computer and sequencer subsystem periodically transmits a time word to the telemetry subsystem via a single buffered channel. This channel is also used to read out the computer and sequencer memory (see Figure N-5).

In the general-purpose computer approach, additional data such as the spacecraft attitude could be transferred from the computer subsystem

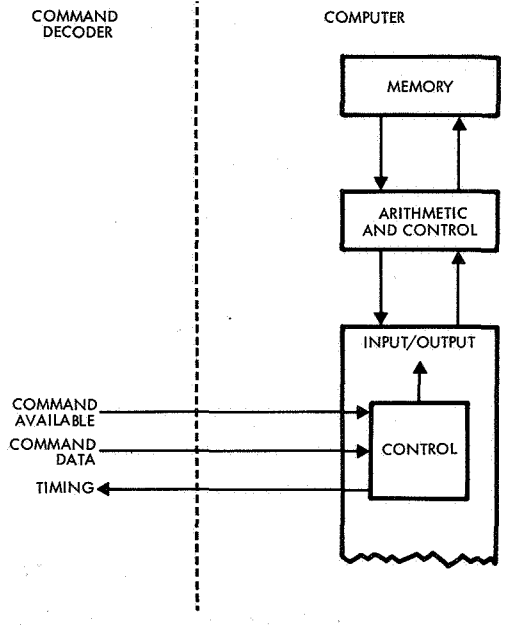


Figure N-4. Computer Interface with Command Decoder

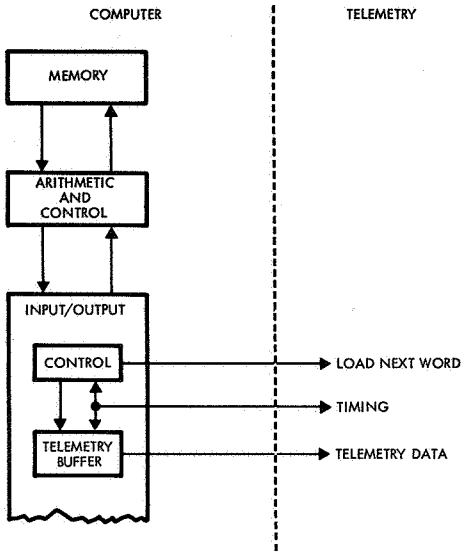


Figure N-5. Computer Containing a Telemetry Buffer Register and Control

to the telemetry subsystem. A second possibility would be to allow the computer to select the channel to be sampled, instead of using a single fixed format, or a relatively small group of formats allowed by a fixed wired counter. One thousand memory words would be required for this function, and provisions should be made for independent access to the computer memory. The addresses must be outputted at a rate of one each 100 microsecond. Some provision must also be made for backup multiplex control in case both computers fail.

Direct memory access would increase the computer equipment by 50 modules, and increase the power required by 0.4 watts. It is recommended that a further study be performed to evaluate the tradeoff of the variable format's advantages versus the increased size of the computer memory.

4.5 Science Subsystem

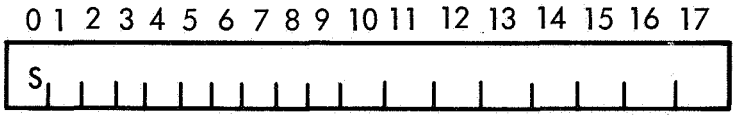
Presently, the computer and sequencer subsystem provides all the necessary timing and sequencing signals for the science subsystem. The formatting and recording of the data for the science subsystem is performed by the telemetry subsystem. The computer can and will provide the same timing and sequencing data. The formatting of scientific data would remain the same because of the high data rate.

Additional use of the computer, such as data compression for the science subsystem is difficult to predict without a detailed knowledge of the experiments to be carried.

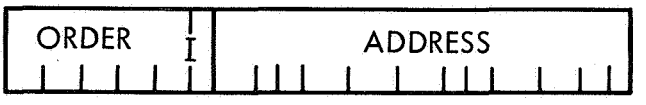
5. DESIGN DESCRIPTION

5.1 Instruction and Data Format

The instruction and data words for the digital computer are each 18 bits in length. Data words are binary, with negative numbers represented as the two's complement of their absolute values. The most significant bit in a word is thus the sign bit. The bits are numbered in order of decreasing significance, so that the value associated with bit n is 2^{-n}. Data word format is illustrated below:



The instruction word is divided into two parts, an order and an address. The least significant order bit (bit position 5) is used to indicate address modification or "indexing." A typical order has the following format:



In the two versions of the LM computer, address modification affects the least significant bits only. The effective address has a "1" in one of the least significant 3-bit positions if either the original address or the index register has a "1" in the corresponding bit position.

In the computer with registers stored in memory, the whole address is affected by the address modification. The effective address is the sum of the twelve bits of the address and the contents of the index register.

5.2 Repertoire of Instructions

A list of instructions and the associated execution time for the two LM/AEA computers are given in Tables N-1 and N-2. A list of instructions and the execution time for the simple parallel computer is given in Table N-3.

Table N-1. LM AEA Instruction Set

	Arithmetic Instructions	Microseconds
ABS	Absolute Value of Accumulator	16
ADD, ADZ	Add to Accumulator	5
CØM	Complement Accumulator	16
DVP	Divide	68
MPR, MPZ	Multiply and Round	65
MPY	Multiply	65
SUB, SUZ	Subtract from Accumulator	5
	Register Operations	
ATX	Address to Index Register	13
CLA	Load Accumulator	5
LDQ	Load Q Register	8
STØ	Store Accumulator	8
STQ	Store Q Register	8
	Shift Instructions	
ALS	Accumulator Left Shift	3N + 13
LLS	Long Left Shift	3N + 13
LRS	Long Right Shift	3N + 13
	Transfer Instructions	
TIX	Transfer and Decrement Index	5
TMI	Transfer on Minus Accumulator	5
TOV	Transfer on Overflow	5
TRA	Unconditional Transfer	5
TSQ	Transfer and Set Q Register	11
	Other Instructions	
INP	Input Data to Accumulator	16 or 67
OUT	Output Data or Discrete	13
DLY	Delay	-

Table N-2. Comparison of Execution Time for Serial and Parallel Versions of LM/AEA Computer

Instruction	Serial	Parallel
ABS	22	16
ADD	22	5
CØM	22	16
DVP	347	68
MPR, MPZ	209	65
MPY	191	65
SUB, SUZ	22	5
AXT	3	13
CLA	22	5
LDQ	22	8
STO	22	8
STQ	22	8
ALS	39 - N	3N + 13
LLS	3 + N	3N + 13
LRS	39 - N	3N + 13
TIX	3	5
TMI	3	5
TDV	3	5
TRA	3	5
TSQ	22	11
INP	22	16 or 67
OUT	22	13
DLY	-	-

Table N-3. Parallel Computer with Registers in Memory Instruction Set

	Arithmetic Instructions	Microseconds
AD	Add to Accumulator	12
DV	Divide	196
MU	Multiply	190
SU	Subtract	12
	Register Operations	
CA	Load Accumulator	10
SA	Store Accumulator	10
SI	Load Index	10
SM	Store Counter	10
	Shift Instructions	
FL	Full left Shift	8 + 8Y
FR	Full Right Shift	8 + 8Y
	Test Instructions	
CØ	Compare Accumulator with Storage	19
	Transfer Instructions	
IT	Index Transfer	12
NT	Negative Transfer	8
ØT	Overflow Transfer	6
TA	Indirect Transfer	8
UT	Unconditional Transfer	6
	Other Instructions	
FS	Full Stop	24
ID	Input Data	10
IN	Input Discrete	10
NØ	No Operation	6
ØD	Output Data	50
ØU	Output Discrete	50

5.3 Computer Implementation

Two possible mechanizations of a computer have been considered for this study. The first is to use integrated circuits and a memory being developed for a current TRW computer. A plated wire memory which is being developed by TRW also has been considered. An alternative possibility is the use of an all-magnetic logic system presently being developed by a TRW research project. This magnetic system is not yet fully developed, but should be available for a 1973 mission. It has the advantage that it is highly resistant to radiation, which might be an advantage for some possible follow-on missions. Magnetic devices have a higher inherent reliability than semiconductors, so that a longer mission might be practical using this type of equipment. Alternatively, a single magnetic computer might replace two semiconductor machines with no sacrifice in system performance.

On the other hand, the uncertainties involved in any research effort increase the risk of a development program, so only semiconductors and core memories have been used in the conceptual design. Since power will be in short supply, a family of low power circuits has been selected. These circuits include NAND gates and a master-slave flip-flop. Each computer is designed to use the selected circuits, and number of modules and power computed for each model.

All designs covered by this study use approximately the same instructions, differing only in power consumption and execution times for the various instructions. These are listed in the foregoing section.

The computer memory is a three-dimensional, coincident-current device capable of one complete memory cycle in two microseconds. Any word in the memory may be either a NDRO or DRO word, depending on the wiring of the magnetic core stack. The logic design of each machine allows for up to 4096 words to be directly addressed. Thus, the computer memory could be doubled from the present design value with no logic changes.

5.4 Computer Input/Output

The computer subsystem input/output accepts serial messages via the command subsystem that have been transmitted from the ground. The format for the computer subsystem input from the command subsystem is as indicated below.

1	2	13 14	31
(1)		(12)	(18)
Class		Address	Data

Class	Address	Data Destination
0	1	Accelerator Counter No. 1
	2	Accelerator Counter No. 2
1	0-4095	Memory Storage (including timers)

The input/output unit of the computer subsystem includes an 18-bit buffer for use with the telemetry system. Data may be shifted into this register from the computer's accumulator. A telemetry signal is used to indicate to the computer that the contents of the register have been sampled.

While the buffer register is being read by the telemetry system, its data are recirculated. One complete computer word would be transmitted as three successive telemetry words, with the remaining bits, if any, filled with zeros. Attitude control and time computation require about 25 percent of each second, so the maximum data readout rate would be of the order of 1600 words/sec.

When the telemetry buffer register is used to transfer elapsed mission time, it can be loaded from the computer once each second. When memory dump is being executed, the register must, of course, be loaded as fast as the data can be accepted (about one word each 465 microsecond), except while the computer is otherwise occupied.

Since the computer must work in a baseline spacecraft, the decode matrix and associated output amplifiers for the discrete input/output system are the same as those used by the sequencer which the computer

would replace. This discrete input/output system will be driven by the computer address register when an "output discrete" order is given.

Similar design philosophy is used in case of serial data inputs and outputs. The discrete matrix is used to activate the selected data channel, and a clock is transmitted to the input source or output destination to control shifting of data.

5.5 Software

Verification of computer programs can be substantiated by designing and effectively using interpretive computer simulations (ICS). An ICS is a program that performs the simulation of one computer on another computer. Either a word-by-word, bit-by-bit or a hybrid technique of simulation can be performed. Program verifications, computer and system test programs, integration and calibration routines, prelaunch and postlaunch simulations and diagnostic programs among others may be simulated. Repeatability of results, ease in performing a multitude of tests and the capability to extract more data utilizing a simulation program are advantageous over running tests on the actual computer. The restriction of the actual computer hardware being available for program checkout is eliminated, providing more time for hardware design and development.

Diagnostic routines will be developed to evaluate the status of the various computer subsystem units. The memory, central processor, and input/output will be exercised to detect any deviation from the nominal operating state.

6. SUBSYSTEM RECONFIGURATION AND FAIL-SAFE CONSIDERATIONS

The computer subsystem will consist of an operating computer and an identical backup computer. Each computer will have its own memory unit, input/output unit, central processing unit, and power regulator. The computer subsystem will also include a central timing unit and a monitor and control unit (MCU).

During the maneuver operation, the two computers will be turned on at the same time and will execute the same program simultaneously. Furthermore, they will operate in synchronism word for word and bit for bit. The results from the arithmetic units of the two computers are

compared serially between the two computers. Also, the discrete command addresses and the serial output from both computers are compared before an output is sent.

If the computers have passed the comparison test, the discrete address and the serial output are transferred to the command decoder. If the comparison test has failed, the output will be temporarily withheld and the computers will be notified to initiate diagnostic testing. The results of the testing from both computers are transferred to the monitor and control unit (MCU) and are compared with the correct known result generated by a shift register in the MCU (Figure N-6). Majority voting determines which one of the three units has failed. It is reasonable to assume that only one of the three units will fail at a time. If one of the two computers has failed, the MCU will set a discrete which can be sampled by the surviving computer. At the same time, the computers calculate the time to insure that the discrete will be received within a nominal period. One must assume that only the surviving computer can keep the correct time. Upon sampling of the discrete, the surviving computer will send an acknowledge signal to the MCU. This acknowledge signal will initiate a reconfiguration sequence which will isolate the failed computer. The switching signal will be transmitted as a part of real-time engineering data to the ground. The ground will acknowledge with approval or with overriding reconfiguration commands.

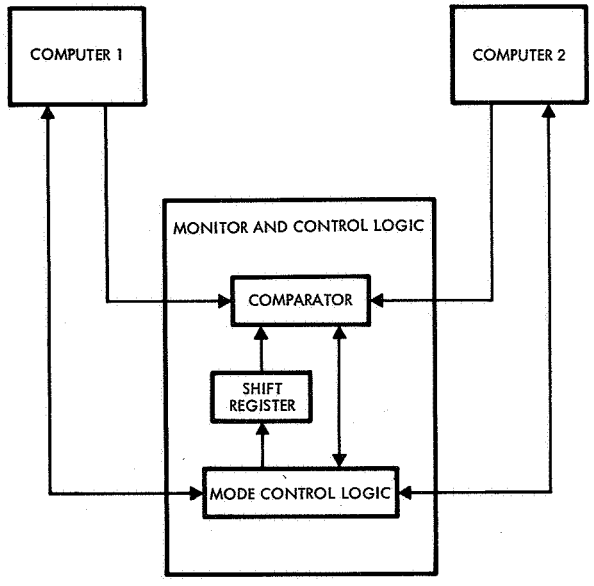


Figure N-6. The Monitor and Control Unit

Since the computer that has failed the comparison test may not be able to successfully complete the diagnostic program, the MCU will keep track of the time required by the computer to complete the diagnostic program. If a computer fails to send the results of the diagnostic program within the set time, the MCU will assume that it has failed and should be switched out of the system. To further insure that the MCU is making the correct decision, the computers can communicate directly via their I/O units. This direct link provides additional testing of each computer by the other computer.

So far, the possibility of a failure in the MCU has not been considered. The MCU is a relatively simple device implemented with a limited number of integrated circuits. Therefore, the reliability of a nonredundant MCU is quite high. A preventative measure is to increase the reliability of this unit by introducing redundancy such as triple-modular-redundancy (TMR) or quadded redundancy. The advantage of the TMR approach is that the fault correction is inherent and instantaneous and no switching is required. The cost of TMR implementation is also lower than that of quadded logic. However, the power consumption and the weight of TMR, though very small, are more than triple those of the nonredundant unit.

When the MCU has failed, a corrective action can also be taken. Under the assumption that only one of the three units can fail at a time, it is assumed that two computers are working. Therefore, they can communicate successfully via the intercomputer link to verify that both are in good condition. The operating computers can either together initiate a reconfiguration sequence to switch the MCU out and then inform the ground, or to inform ground first and let the ground initiate a reconfiguration sequence.

If the MCU failed after successfully detecting a comparison failure, the ground can be used as a backup for the MCU. It is done by setting a flag which will be transmitted to the ground at the beginning of the diagnostic program as a real-time engineering data. The ground will count the time and compare with the known successful completion time. If the

MCU has failed during this period and cannot set a flag in a nominal time to signal a successful completion, then the ground can assume that the MCU has failed.

From a power consumption point of view, it is desirable in some phases of the space flight to turn off the power to one computer and to operate in the sequential mode. The primary computer will remain on until it has failed. Then the second computer will be switched in. The MCU will remain operating until a failure has been detected. Under normal conditions, the operating computer will periodically exercise and test the MCU by sending the diagnostic program result to MCU for testing. The MCU will acknowledge successful comparison within a set time, or indicate a diagnostic error. If the MCU fails to respond in this period, it is assumed that the MCU has failed.

There are several possible failure modes. If the MCU has not initiated any erroneous switching action, the primary input/output unit is working and the second computer remains off. The primary computer can inform the ground to take necessary action. If the MCU has erroneously initiated some switching such that both the primary I/O unit and the second computer are on or off at the same time, or the primary I/O unit is off and the second computer is on, the ground can detect this abnormal condition by examining the engineering data and/or interrogating both computers.

The operating computer will also periodically execute the confidence test and the diagnostic test and compare the result with the known result. At initiation, the computer will inform the MCU that testing has begun. It will also report to the MCU at the end of a successful test. If the computer fails to initiate the test on time or fails to report the completion of the test within a set time limit, the MCU will set a flag which will be transmitted to the ground as a real-time engineering data. The ground can request a memory dump for further diagnosis.

In order to avoid erroneous output from a failed computer, the MCU, upon successful detection of a primary computer failure, will turn off the primary input/output unit. Also, in order to avoid the time delay due to propagation time between the spacecraft and the ground, the MCU will

turn on the power for the second computer. The change of status of these two units will be transmitted to the ground as real-time engineering data. The ground can either approve or override this decision. Under the assumption that the probability of simultaneous failures of the primary computer and the MCU is negligibly small, the MCU will successfully turn off the primary computer and turn on the second computer. Should the other three possible cases occur, that is, should both units be on, or both off, or the primary input/output on and the second computer off, the ground will be able to detect this inconsistency from the engineering data, and can initiate appropriate corrective action such as switching both the primary computer and the MCU off and starting up the second computer.

It is to be noted that cross-strapping of the input/output units to the two central processing units has been considered. A detailed reliability analysis is given in the next section. The foregoing considerations remain the same with cross-strapping. The term primary input/output unit simply means the one which is operating with the primary central processing unit.

7. RELIABILITY ANALYSIS

The reliability estimate for the computer subsystem is based on the following assumptions:

- Mission duration is 6800 hours
- Time to failure is exponentially distributed
- Failure rate of nonoperating equipment is zero
- Parallel equipment is operating at all times
- Reliability of the relatively simple cross-strapping circuitry is high as compared with various functional units, and is assumed perfect in this study.

Table N-4 lists the components, the failure rates and the computer reliability for the 6800-hour mission.

Since no firm reliability requirement has been established for the computer subsystem, several subsystem configurations have been considered to give a reliability range of 0.943 to 0.980. The various subsystem configurations and the corresponding reliabilities are summarized

Table N-4. Individual Component Reliabilities

Component Name	Failure Rate (λ) (bits/10^9)	Probability of Success (R) 6800-hr Mission	Probability of Failure Q = 1-R
Central Timing Unit	630	0.99572	0.00428
Input/Output Unit	13,320	0.90942	0.09058
Input Decoder	2,430		
Output Decoder	9,210		
Telemetry	1,680		
2048 Word Memory	12,875	0.91355	0.08645
Central Processing Unit	10,110	0.93360	0.06640
Monitor and Control Unit	450	0.99694	0.00306

in Table N-5. Detailed analyses for these configurations are given in Figures N-7 through N-15. As expected, the subsystem reliability increases as more redundancy and cross-strapping is added. This does not mean that the optimum configuration is the one with the highest reliability. Tradeoff analyses between reliability, cost, weight, power, and other parameters must be effected before an optimum configuration can be selected.

Table N-5. Reliability Estimates for Various Computer Subsystem Configurations

Configuration		Calculated Reliability
A. Serial System		0.772
B. Redundant Computers	On-line	0.943
	Standby	0.963
C. Redundant Computers, Cross-strapped Memories		0.963
D. Redundant Computers, Majority Voting Clocks		0.947
E. Redundant Computers, Cross-strapped Memories, Majority Voting Clocks		0.967
F. Redundant Computers, Cross-strapped Memory and I/O, Majority Voting Clocks		0.977
G. Redundant Computers, Majority Voting Clocks and Comparators		0.950
H. Redundant Computers, Cross-strapped Memories, Majority Voting Clocks and Comparators		0.970
I. Redundant Computers, Cross-strapped Memories and I/O, Majority Voting Clocks and Comparators		0.980

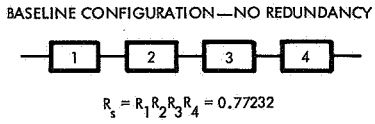


Figure N-7. Serial Configuration

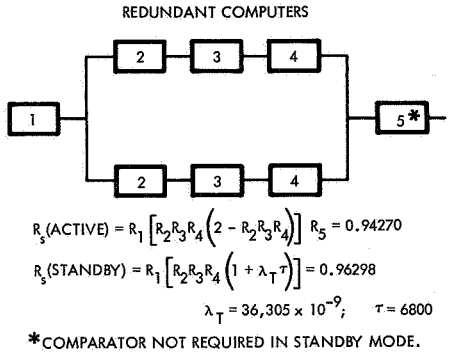


Figure N-8. Redundant Computers - Single Computer Consists of Arithmetic, I/O and Memory Units

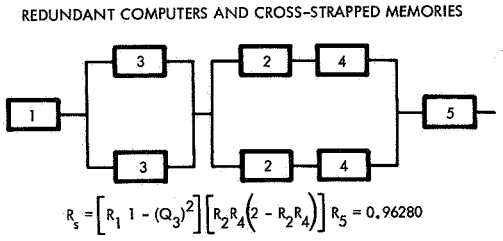


Figure N-9. Redundant Computers and Cross-Strapped Memories

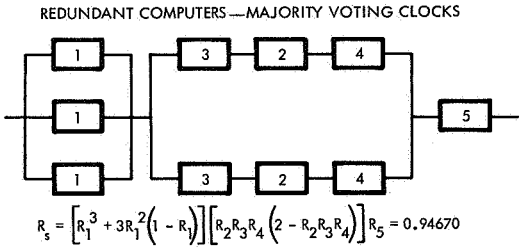


Figure N-10. Redundant Computers - Majority Voting Clocks

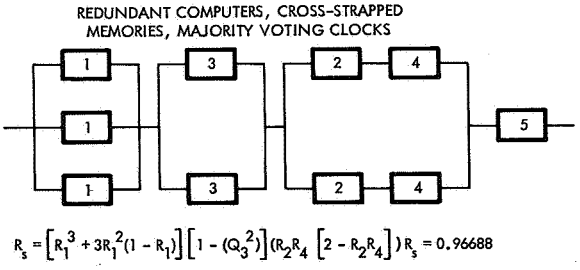
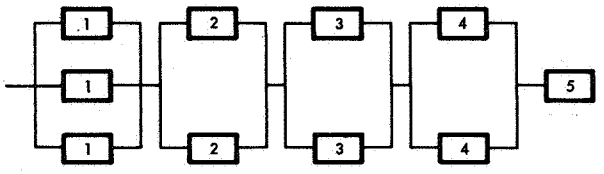


Figure N-11. Redundant Computers, Cross-Strapped Memories, Majority Voting Clocks

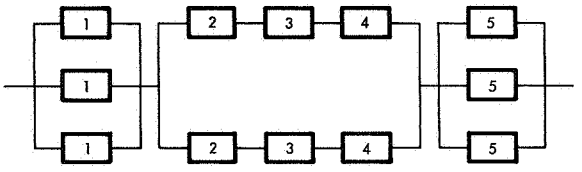
REDUNDANT COMPUTERS, CROSS-STRAPPED MEMORIES AND I/O, MAJORITY VOTING CLOCKS



$$R_s = \left[R_1^3 + 3R_1^2(1 - R_1)\right]\left[1 - (Q_2)^2\right]\left[1 - (Q_3)^2\right]\left[1 - (Q_4)^2\right]R_5 = 0.97699$$

Figure N-12. Redundant Cross-Strapped Computers, Majority Voting Clocks

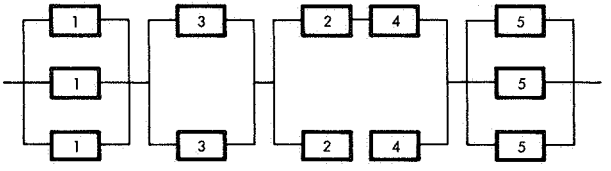
REDUNDANT COMPUTERS, MAJORITY VOTING CLOCKS AND COMPARATORS



$$R_s = \left[R_1^3 + 3R_1^2(1 - R_1)\right] R_2R_3R_4\left[2 - R_2R_3R_4\left[R_5^3 + 3R_5^2(1 - R_5)\right]\right] = 0.94958$$

Figure N-13. Redundant Computers, Majority Voting Clocks and Comparitors

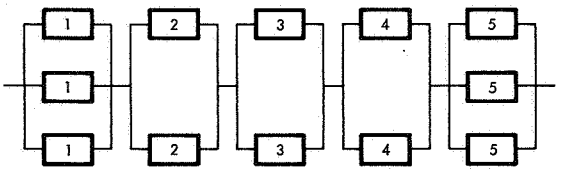
REDUNDANT COMPUTERS, MAJORITY VOTING FOR CLOCK AND COMPARATOR, CROSS SWITCHED MEMORIES



$$R_s = \left[R_1^3 + 3R_1^2(1 - R_1)\right]\left[1 - (Q_3)^2\right]\left[R_2R_4\left[2 - R_2R_4\right]\right]\left[R_5^3 + 3R_5^2(1 - R_5)\right] = 0.96982$$

Figure N-14. Redundant Computers, Cross-Strapped Memories, Majority Voting Clocks and Comparitors

REDUNDANT COMPUTERS, MAJORITY VOTING FOR CLOCK AND COMPARATOR, CROSS SWITCHED MEMORY AND I/O



$$R_s = \left[R_1^3 + 3R_1^2(1 - R_1)\right]\left[1 - (Q_2)^2\right]\left[1 - (Q_3)^2\right]\left[1 - (Q_4)^2\right]\left[R_5^3 + 3R_5^2(1 - R_5)\right] = 0.97996$$

Figure N-15. Redundant, Cross-Strapped Computers, Majority Voting Clocks and Comparitors

8. FUTURE APPLICATIONS

This section of the study enumerates some potential functions which merit additional investigation for future digital computer implementation.

8.1 Digital Control System

The present control system is basically an analog system. An integrated digital computer control system would close some additional control loops to provide for more precise control. Optimal use of redundant sensors can also be incorporated in the integrated digital control system.

8.2 Navigation

Kalman filtering techniques could be used for smoothing and predicting sampled data for solution of the guidance and navigation problems. Backup mode of navigation based upon valid information prior to data dropout could be incorporated into the computer until restoration of valid input data or command from the ground.

8.3 Data Compression

The amount of raw data from the science experiments will pose a tremendous requirement on the data storage, telemetry and communication systems. Various techniques for redundancy removal in the raw data by use of a digital computer merit additional investigation.

8.4 On-Board Diagnosis and Switching

A digital computer can provide for status checking, diagnosis and switching of other subsystems. The selection of an alternative path could be handled by a computer decision. The computer can also provide the ground with the information for a decision. Ground commands would still be able to override the on-board digital computer.

Of course, these additional tasks require additional data processing capability. A new computer design may be required if portions or all of these functions are to be implemented. It also necessitates a high degree of reliability and confidence in the digital computer.

APPENDIX P

SCIENCE DATA AUTOMATION EQUIPMENT VERSUS INTEGRATED COMPUTER AND SEQUENCER UNIT

The data automation sequencer (DAE), as a separate unit, was conceived as a means of providing control flexibility to a variety of scientific instruments which would be assigned to the spacecraft on a mission basis. A tradeoff study revealed that by adding a timer (Science timer) and increasing the command output capability (256 to 512) of the computer and sequencer unit proposed in Voyager Task B of Phase 1A, sufficient command functions for scientific instrument control could be provided while maintaining the desired flexibility. Further, since many operations performed within the DAE sequencer duplicated those performed within the computer and sequencer, significant savings in hardware are realized by combining the functions into a single unit.

In the recommended computer and sequencer unit, a block of stored program commands is provided for the science experiments. The sequence of execution of the commands is controlled by the science timer as well as the orbit and maneuver timers. Functions performed by individual commands are defined by the instruments to which they are connected and the required timing of execution of the commands is accomplished by programming.

A section of the computer and sequencer command decode matrix which produces commands for experiments is remotely located in the planetary scan platform. The remote decode unit (RDU) operates as if it were an integral part of the computer and sequencer. This technique enables a fixed interface between the computer and sequencer and the planetary scan platform consisting of relatively few signals, while experiment control signals need only be patched into the RDU output.

From a hardware standpoint, by combining the DAE sequencer functions into the computer and sequencer, there is a net reduction of approximately 30 percent of the components under what would be

required if the units were implemented separately. In terms of effect on system reliability, a serial DAE would cause a reliability decrease of 0.08 as compared with the single unit. Hence, the combined functional capability in the computer and sequencer as described is recommended.

APPENDIX Q

BATTERY TRADEOFFS

A study to determine the optimum battery to accomplish the mission was undertaken, based on a representative set of requirements for a Voyager-Mars mission consisting of an eight-month transit phase and a six-month orbiting phase. Transit phase consists of up to six battery discharges with a maximum discharge requiring 1252 watt-hours. The orbiting phase may consist of up to 300 charge/discharge cycles with a maximum discharge requirement of 1205 watt-hours if the eclipse season does not exceed 120 cycles. The orbit period is 13.5 hours, providing a minimum of 11.2 hours for battery charging.

The battery types considered are presently developed for space applications. These are silver-zinc, silver-cadmium, and nickel-cadmium. These three types were compared with respect to magnetic properties, life, energy density, and reliability. Various battery configurations were compared and calculations performed for battery cell sizing and battery system reliability.

1. ENERGY DENSITY

An initial comparison of the three battery types was made on the basis of energy density. Partially achieved battery energy density values for the three types are listed in Table Q-1.

Table Q-1. Energy Densities of Three Types of Batteries

Silver-zinc	30 to 50 watt hours/pound
Silver-cadmium	20 to 30 watt hours/pound
Nickel-cadmium	12 to 16 watt hours/pound

These values include battery cell weight and an estimated packaging factor. They represent the energy obtainable from full charge and 100-percent depth of discharge.

2. USEFUL BATTERY LIFE

The 14-month Voyager-Mars mission requires approximately 65-percent charged-stand time and 35 percent charge/discharge cycling. Because of wearout characteristics of battery cell components, each type of battery has an inherent useful life limit. This limit will vary depending on the type of application and the relative amounts of cycling and charged stand. Estimated useful life limits for the Voyager mission are shown in Table Q-2.

Table Q-2. Useful Life Limits for Three Types of Batteries

Silver-zinc	15 months
Silver-cadmium	18 months
Nickel-cadmium	Greater than 36 months

3. CYCLE LIFE

Within the limits of useful battery life, the number of charge/discharge cycles of a given energy output that may be obtained is a function of the depth of discharge of the battery, i.e., the discharge energy as a percentage of nominal battery capacity. For this reason, none of the three battery types is operated at 100-percent depth of discharge in applications requiring repeated cycling. Repeated charge/discharge cycling causes degrading effects on capacity to different degrees on each of the three types. In general, deep cycling of the silver-zinc and silver-cadmium battery types causes loosening and migration of the active materials in the battery cells, resulting in reduced cycle life. Cycling of a nickel-cadmium battery gradually alters the structure of the battery cell electrodes, resulting in a reduction of available discharge energy. Table Q-3 shows the approximate number of cycles obtainable from each type of battery for several values of depth of discharge.

The values in the table represent the number of cycles to reach a prescribed under-voltage limit. The cycle numbers shown are somewhat lower than those usually found in the literature because they reflect operation of a complete battery as opposed to a single cell or a cell pack. For the silver-zinc and silver-cadmium batteries, the degradation in performance due to cycling is not recoverable. For nickel-cadmium batteries,

Table Q-3. Number of Charge/Discharge Cycles Obtainable at Selected Depths of Discharge

Depth Discharge	Silver-Zinc	Silver-Cadmium	Nickel-Cadmium
10	2000		10,000
20	1000	5000	10,000
25	500	2000	5,000
33	200	1000	2,000
40		500	1,000
50			500
60			200

the degradation represents a loss in capacity which is largely recoverable by the process of battery "reconditioning." Reconditioning is performed by subjecting the battery to a low-rate discharge through a fixed load to a selected voltage value and then recharging. This will return available battery capacity to its initial value. Reconditioning has been employed on earth satellite programs and will be used on the Voyager nickel-cadmium battery.

To satisfy the cycling requirements of the basic 14-month, 300-cycle Voyager mission, the recommended depth of discharge values given in Table Q-4 have been selected from Table Q-3.

Table Q-4. Recommended Depth of Discharge for Each Battery Type

Silver-zinc	25 percent
Silver-cadmium	40 percent
Nickel-cadmium	50 percent

When the energy density values are modified by the depths of discharge shown in Table Q-4, the resultant battery weights may then be compared for relative merit.

To support upgraded Voyager missions of up to 30 months, the useful life limit rules out silver-zinc and silver-cadmium batteries. A nickel-cadmium battery could be used at a 50-percent depth of discharge or deeper if the number of continuous cycles is low and if reconditioning were provided. Without reconditioning, the depth of discharge should be reduced to 40 percent to provide 900 cycles of charge and discharge associated with a longer mission.

4. BATTERY WEIGHT COMPARISON

To compare estimated battery weights for each type of battery, Table Q-5 was generated. It covers the ranges of energy density and depths of discharge used for the three battery types and may be used to select specific examples of battery weights. Calculations were made using a maximum energy requirement of 1205-watt hours, i.e., 524 watts for 2.3 hours during maximum eclipse. Weight values were calculated by use of the following formula:

$$W = \frac{1205}{\frac{(\text{depth of discharge})}{100}\,(\text{energy density})}$$

Table Q-5. Battery Weight for Selected Values of Energy Density and Depth of Discharge

Depth of Discharge (Percent)	Watt-Hours/Pound of Packaged Battery							
	12	14	16	20	25	30	40	50
70	147	126	111	--	--	--	--	--
60	172	148	129	---	--	--	--	--
50	207	177	155	124	99	83	--	--
40	258	221	194	155	124	103	78	62
33-1/3	310	267	233	186	149	124	93	74
25	413	354	310	248	198	165	124	99
	← NiCd →							
				← AgCd →				
						← AgZn →		

Using the selected depth of discharge values shown in Table Q-4, and mid-values for each energy-density range, the comparative battery weights given in Table Q-6 are obtained.

Table Q-6. Comparative Battery Weights

	Depth of Discharge (Percent)	Energy Density (w-h/lb)	Battery Weight (lb)
Silver-zinc	25	40	124
Silver-Cadmium	40	25	124
Nickel-Cadmium	60	14	148
	50	14	177
	40	14	221

5. MAGNETIC CHARACTERISTICS OF ALKALINE BATTERIES

Nickel-cadmium batteries consisting of 22 12AH cells and weighing 32 pounds have an inherent, nonoperating magnetic field of the order of 1 to 2K gamma. Proposed Voyager batteries, approximately 50 pounds each, may have fields one and one-half this value. Operating fields (during charge and discharge) can be adjusted over wide limits by the method of routing of the wiring between cells, from cells to battery connector, and external to the battery. Essentially complete cancellation of induced fields may be approached in this manner.

The nonoperating fields from silver-cadmium and silver-zinc batteries that have been fabricated from nonmagnetic materials are very low. With no attempt to wire these batteries for compensation, magnetic fields during charge and discharge can be of the same order of magnitude as for nickel-cadmium batteries (e.g., 1000 gamma at five amperes). With compensating wiring, reduction in field by a factor of 10 is feasible.

6. BATTERY SELECTION

A nickel-cadmium battery system has been selected as the most suitable for the Voyager-Mars mission. Although the heaviest of those shown, it offers a growth potential in mission life and discharge capacity and the highest reliability. Its capability of being reconditioned to recover lost capacity due to cycling is an added attractive feature leading to its selection. The slightly higher permanent magnetic field does not, at present, seem to represent a significant drawback. Should weight become a significant problem, a silver-cadmium battery with a reliability only slightly lower than the proposed nickel-cadmium battery, but without capability for mission life extension, could be developed for use on the Voyager spacecraft.

The cycle life used for the sizing calculations presented herein represents a combination of two worst cases—one is the longest eclipse and the other is the greatest number of successive cycles. Further analyses have indicated that 2.3-hour eclipses will occur only in a short eclipse season where a maximum of 120 successive cycles between reconditionings would appear. For such a mission a depth of discharge in excess of 60 percent is completely within the battery capability. If the longer eclipse season (300 cycles) is contemplated, the maximum eclipse duration would be considerably below two hours. In such a case, even for the highest power requirements presently known, the discharge would not exceed 50 percent of the battery capacity.

APPENDIX R

SOLAR ARRAY AND BATTERY CONTROL TRADEOFFS

In selecting methods for solar array and battery control, the basic criteria were to achieve high reliability and to make maximum utilization of available power. The general approach towards arriving at the optimum system configuration was to make maximum utilization of the available power from the power sources — solar array and battery — without compromising reliability. Since the power sources are the primary weight contributors, minimizing the power-source requirements will generally provide the minimum weight and volume design of the power subsystem. The power requirements used in the tradeoffs consist of figures available in the early part of the study.

1. CANDIDATE SYSTEMS

Based on the analysis of the power conditioning equipment, load power requirements, solar array, battery and controls, four baseline configurations were established (Figures R-1 through R-4) for tradeoff comparisons.

The scheme shown in Figure R-1 uses a shunt limited to maintain the main bus at 50 VDC during sunlight. A battery boost regulator maintains the bus at 50 VDC during battery discharge.

The maximum power tracker of Figure R-2 draws the maximum amount of power available from the solar array. The main bus voltage varies with the discharge and charge voltage characteristics of the battery.

The buck-boost regulator approach of Figure R-3 is very similar to the maximum power tracking approach except that the solar array operating point is not controlled to the maximum power point of the array.

The design of Figure R-4 brings in a boost regulator whenever the solar array voltage is less than the battery and shunts the array voltage at the end-of-life conditions.

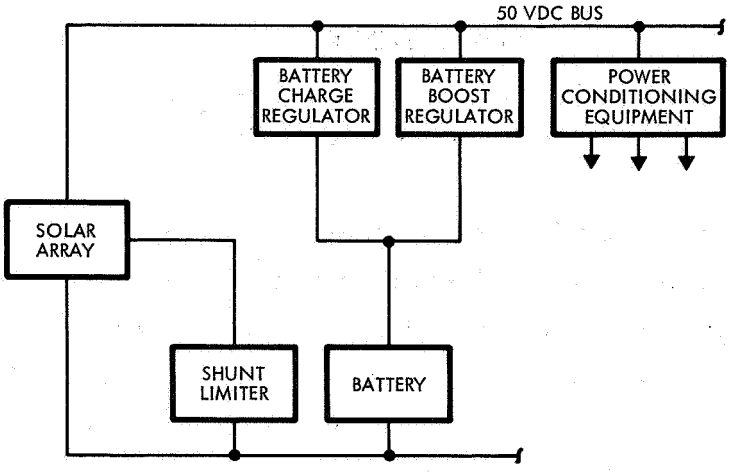


Figure R-1. Shunt Limiter Approach

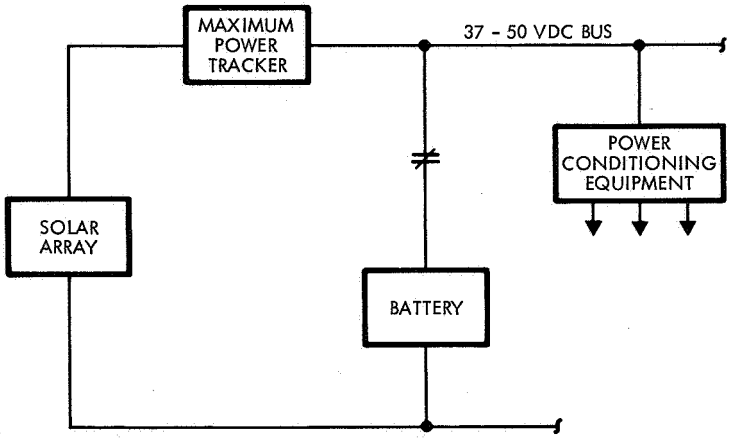


Figure R-2. Maximum Power Tracker Approach

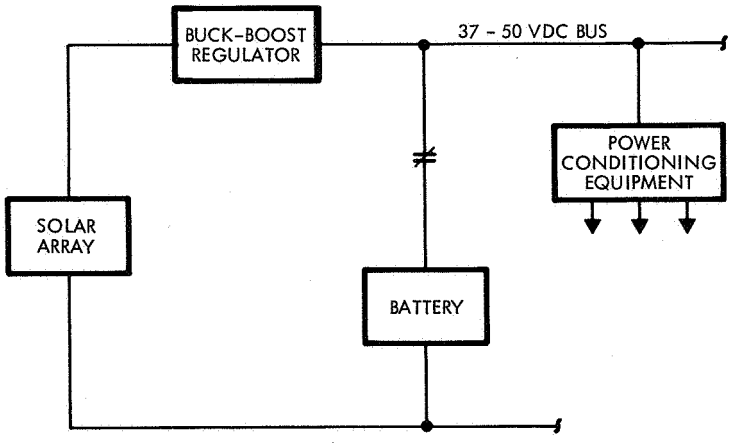


Figure R-3. Buck-Boost Regulator Approach

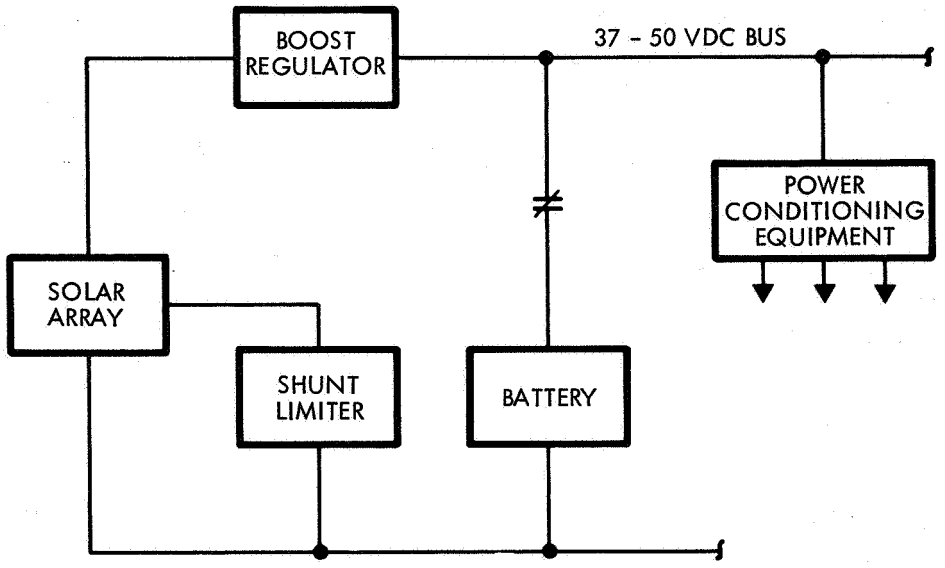


Figure R-4. Boost-Shunt Regulator Approach

2. POWER UTILIZATION COMPARISON

Main bus power and solar array power requirements are tabulated in Tables R-1 through R-4 for Mars orbital operation and Mars encounter for the candidate power subsystem. The assumptions used in the study are as follows:

1) Power requirements obtained from Table R-1

2) The load requirements have been increased (+3 percent) for the unregulated bus configurations due to the additional losses to be incurred in the power conditioning equipment compared to the regulated bus approach.

3) Battery charging power based on battery temperatures of 90°F, parallel charging, nickel-cadmium battery

4) Regulator efficiency data obtained from Third Quarterly Progress Report, PSCR, Report No. E-7441.2-005.

Table R-1. Shunt Limiter Power Requirements (in watts)

	Orbital Operation		Mars Encounter	
	Eclipse	Sunlight	Orbit Insertion	PV Orbit Operation
Load power*	521	485	608	660
Battery energy (watt-hours)	1258		1275	
Battery charging** power		249		136
Main bus power		734		796
Shunt limiter losses		0		0
Solar array requirements at maximum power point***		878		952

* Power conditioning efficiency: 85 percent
** Boost regulator efficiency: 95 percent
*** Power utilization: 38.6 percent

Table R-2. Maximum Power Tracker Power Requirements (in watts)

	Orbital Operation		Mars Encounter	
	Eclipse	Sunlight	Orbit Insertion	PV Orbit Operation
Load power*	537	500	626	680
Battery energy (watt-hours)	1235		1252	
Battery charging power		215		110
Main bus power		715		792
Maximum power tracker losses (N = 0.88)		86		95
Solar array requirements at maximum power point		801		887

*Power conditioning efficiency: 82 percent

Table R-3. Buck Boost Power Requirements (in watts)

	Orbital Operation		Mars Encounter	
	Eclipse	Sunlight	Orbit Insertion	PV Orbital Operation
Load power*	53	500	626	680
Battery energy (watt-hours)	1235		1252	
Battery charging power		215		110
Main bus power		715		790
Buck boost regulator looses (N = 0.87)		93		103
Solar array requirements at maximum power point		808		893

*Power conditioning efficiency: 82 percent

Table R-4. Boost-shunt Power Requirements (in watts)

	Orbital Operation		Mars Encounter	
	Eclipse	Sunlight	Orbit Insertion	PV Orbital Operation
Load power*	537	500	626	680
Battery energy (watt-hours)	1235		1252	
Battery charging power		215		110
Main bus power		715		790
Boost regulator losses		0		
Shunt limiter losses		0		0
Solar array maximum power requirements**		741		830

* Power conditioning efficiency: 82 percent
**Power utilization: 0.95 percent

Table R-5 summarizes the battery and solar array power requirements for the four candidate systems.

Table R-5. Summary of Power Requirements

Candidate System	Battery Energy (watt-hours) Mars Orbital Operation	Solar Array Power at 1.62 AU Mars Encounter (watts)
Shunt limiter	1258	952
Maximum power tracker	1235	887
Buck-boost	1235	893
Boost-shunt	1235	830

Comparing the four approaches, the boost-shunt approach is superior from the standpoint of both minimizing battery energy and solar array power.

3. WEIGHT COMPARISON

Weight comparisons have been made for the candidate systems as tabulated in Table R-6. The following assumptions were made:

1) Weight data based on Third Quarterly Report, PSCR, Report No. E7441.2-005

2) Separate charge and discharge regulators for each of the three batteries

3) Dc/Dc converter weight based on eight individual converters, one for each major power user subsystem

4) Specific weight of solar array: 3.58 watts/pound at 1.67 AU

5) Specific energy of battery: 14 watt-hours/pound

6) Weight differences are depicted in this tradeoff. The 400-Hz inverter, synchronizer supply, telemetry, functions (or weights) would be common to all candidate systems, as such, were not included.

7) Dc/Dc converters for the unregulated bus systems (37 to 50 VDC) are the regulated type.

8) Electronic circuits are nonredundant.

Table R-6. Weight Comparison - Nonredundant Electronics

Item	Shunt Limiter	Maximum Power Tracker	Buck-Boost	Boost-Shunt
Array Control	8	19	27	10
Battery charge control	10.5	3.6	3.6	3.6
Battery boost regulator	8.1	0	0	0
DC/DC converter	13.6	24	24	24
TOTAL	40.2	46.6	54.6	37.6
Conversion equipment weight difference*	+2.6	+9.0	+17.0	0
Battery energy (watt-hours)	1258	1235	1235	1235
Battery weight difference*	+1.4	0	0	0
Solar array power (watts)	952	887	893	830
Solar array weight difference*	+29.4	+11.2	+12.6	0
TOTAL	+33.4	+20.2	+29.6	0

*Lowest weight system gest a zero (0) value.
All unspecified units are in pounds.

Table R-7 is a similar weight comparison but based upon a subsystem utilizing fully redundant electronics.

4. RECOMMENDED SYSTEM

The shunt-boost system is recommended because it uses the least battery energy and solar array power and also has the least weight.

Table R-7. Weight Comparison - Redundant Electronics

Item	Shunt Limiter	Maximum Power Tracker	Buck-boost	Boost-Shunt
Array control	12	38	50	17
Battery charge control	19.5	6	6	6
Battery boost regulator	15.6	0	0	0
DC/DC converter	25.4	48	48	48
TOTAL	72.5	92	104	71
Conversion equipment weight difference*	+1.5	+21	+33	0
Battery energy (watt-hours)	994	975	975	975
Battery weight difference*	+1.4	0	0	0
Solar array power	935	865	872	792
Solar array weight difference*	+29.4	+11.2	+12.6	0
TOTAL	+32.3	+32.2	+45.6	0

*Lowest weight system gets a zero (0) value.
All unspecified units in pounds.

APPENDIX S

AC-VERSUS-DC DISTRIBUTION

A tradeoff study was made to determine the most effective means of distributing electric power within the recommended Voyager spacecraft. The competing systems analyzed are shown in Table S-1.

Table S-1. Weight Comparison

Subsystem Configuration	Weight*(lb)	Efficiency
Regulated AC square wave inverter with individual subsystem transformer-rectifier units	16.2	78.5
Regulated AC sinewave inverter with individual subsystem transformer-rectifier units	15.2	75.5
Centralized converter supplying all subsystems with standardized voltages	11.9	79.6
Unregulated DC main bus with individual sybsystem DC to DC converters	13.4	80.0

*Excluding cable harness weights.

As can be seen, no one system has a distinct advantage over the others. Thus flexibility, reliability, cable weight, EMC, and fault isolation become overriding considerations in the selection of the preferred approach. From an EMC standpoint, the weight savings for interference filters and cable shielding using a DC system opposed to square-wave AC was calculated to be 6.9 pounds. In addition, our experience shows that use of the DC distribution configuration will result in much less intrachassis interference than would the use of the square wave AC configuration.

For the above reasons, the recommended power distribution system is an unregulated DC main bus with individual subsystem DC-DC converters.

APPENDIX T

WIRING INTEGRATION DESIGN ENGINEERING

The interconnection of spacecraft systems at TRW has been made easier, more exacting, and less costly by use of machine and computer handled wiring data. This concept has been termed wiring integration design engineering (WIDE). In using this concept, every wire and end connector comprising the cabling will be listed on a standard TRW form. This form, when filled out, documents wire type, input and output pin assignments, signal description, signal parameters, and identification of the signal within a given subsystem. This form can be handled by data handling equipment, with subsequent procedures being performed semi-automatically. A few of the major advantages of this approach are:

- Accurate and rapid handling of the many individual small bits of data and information which go together to define electrical distribution hardware interfaces.
- Automatic error detection. Errors are minimized because the machine can detect errors.
- Minimizing of schematics and typed wire lists.
- Speed. All functions are initiated and completed more rapidly. The initial transferral onto cards can be done by a keypunch operator faster than by a draftsman.
- Ease of incorporating changes and maintaining document control.
- Providing a standard language for all internal interfacing subsystems and subcontractors.

In practice, WIDE uses a single, 80-column data handling card to define the interface between two connected points in a system (point-to-point wiring). Standardized codes, abbreviations, and literals are employed in a given format to describe where a wire comes from, where it goes, its type and size, and the type, characteristics, and designation of the signal on the wire.

Thus, the basis for the WIDE system is that a single card, or tape data word frame, represents a connection or potential connection for one end of a wire, such as a connector pin or terminal. If this connection is

not to be used, it will then be stated on the single card which will remain in the system. However, if the terminal is to be connected, the card represents one end of a wire, which is defined as a single, continuous, and unbroken length of an electrical conductor having two, and only two, ends. The card format specifies this end in the "from" columns and the other end in the "to" columns. Since every termination, potential or otherwise, is specified in the "from" columns, and since all wires have two and only two ends, the completed data package will contain two cards for every wire, one a mirror image of the other, called a "matched pair." This is the basis for several important aspects of WIDE, particularly error checking.

1. IMPLEMENTATION

The general flow diagram for the sequence of WIDE operations is shown in Figure T-1. As a wire is defined and the ends are verified as being correct, an identifying number is assigned, the best description is chosen, and a pair of cards, each the exact mirror image of the other, is produced and collated into the master tape or card deck. The process then becomes continuing——each "wire" is verified, description is standardized, code number is assigned, and then collated into the master in the proper sequence while automatically removing the old card or frame. This process continues until all cards either show "no connection" or have a code number assigned and constitute a matched pair.

The process is verified by producing two tab runs from the same tape or card deck. The first, or pin sequence tab run will list every pin by sequence in every connector, or every terminal by sequence on every terminal board, and will have either "no connection" or a valid code numbered wire. The second, or matched pair listing uses the same data, sorted by the wire code number, which will then list sequentially two mirror image cards for every wire, with the "no connection" cards following at the end.

At any given time in the development, the above two listings can easily be made from the master tape or deck and all exceptions spotted easily, thereby defining the work area remaining to the electrical distribution engineer.

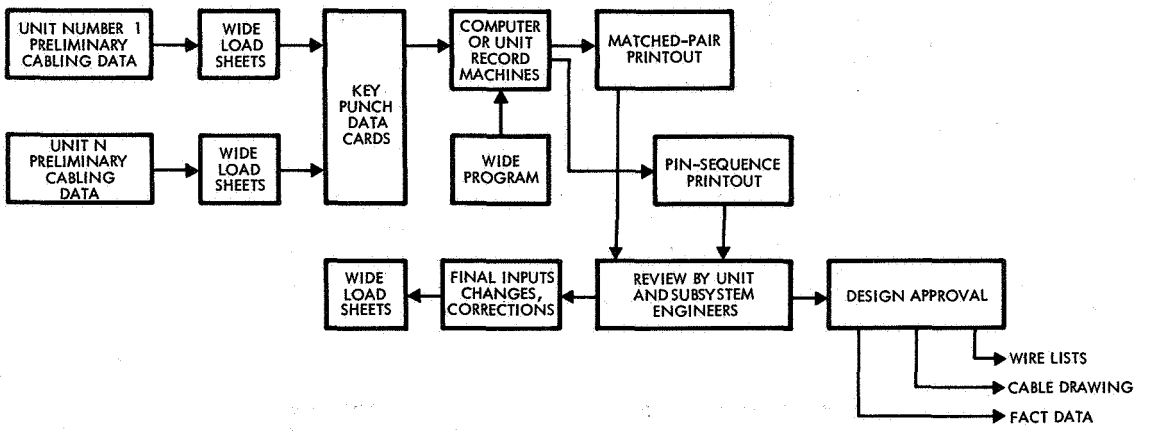


Figure T-1. WIDE Sequence Flow Diagram

2. FACT PRINTOUT

The flexible automatic circuit tester (FACT) is a preprogrammed data card controlled means of automatically testing cabling. The WIDE data card format has been developed to be compatible with FACT requirements. The capability for an automatic, computer-controlled transition from a WIDE data deck to a FACT data deck has been incorporated. Both the WIDE and FACT card formats employ identical data in approximately 50 percent of the data fields; each format contains data peculiar to itself in the remaining 50 percent of the data fields.

A FACT deck can be obtained as a computer output by providing a WIDE pin-sequence card deck and a FACT computer program. The WIDE data fields not required by FACT are rejected, and by operating on the balance of the data, the cards required to control the FACT machine are directly produced. The flow diagram for the FACT sequence of operations is shown in Figure T-2.

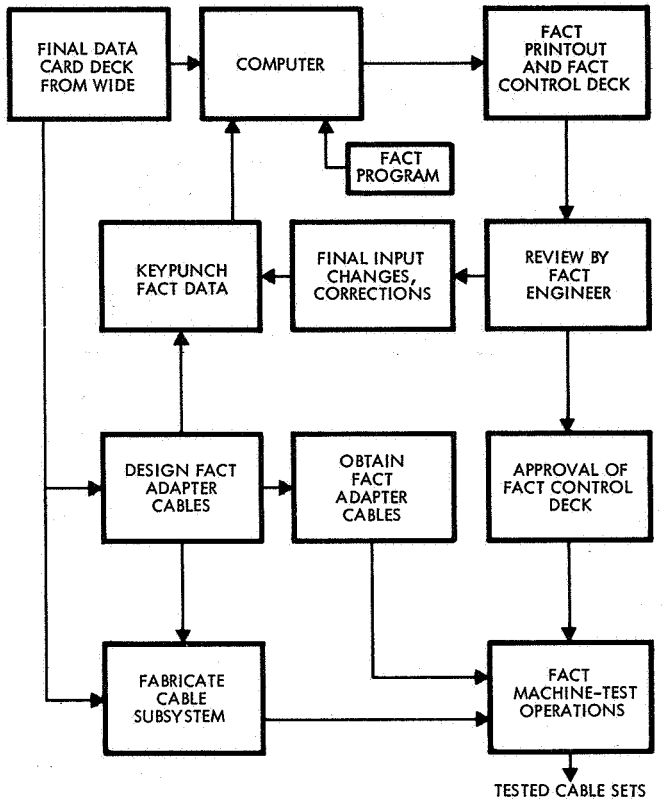


Figure T-2. FACT Sequence Flow Diagram

APPENDIX U
PYROTECHNIC TRADEOFFS

1. SOLID STATE VERSUS RELAY CIRCUITRY FOR PYROTECHNIC CONTROL

A preliminary reliability evaluation of two alternate ordnance firing circuits was performed. The relay firing circuit is illustrated in Figure U-1. The solid state ordnance firing circuit is illustrated in Figure U-2. These two circuits are essentially identical except that circuit 1 employs a momentary relay to fire the ordnance while circuit 2 employs a silicon controlled rectifier to perform the function.

A comparison of characteristics of the two circuits is presented in Table U-1. Available data provides an estimate that the relay failure rate is 170 per billion hours and the actuation failure rate is 12 failures per billion actuations. This can be compared to a Voyager predicted failure rate of 450 failures per billion hours.

The existing orbital data on silicon controlled rectifiers is limited to 1.76 million hours with no failure, resulting in a calculated failure rate of 520 failures per billion hours at 60 percent confidence.

The predominant failure modes of the relay are coil open and shorts, premature relay closing due to vibration and failure to close due to foreign particles on the contacts.

Redundant relays or firing circuits could protect against shorts, opens and failures to close. Premature closing due to vibration should not be a serious problem since circuit arming occurs during cruise phases of the mission, when vibration levels should be minimized. Momentary contact closure during times when the circuit is not armed will not result in premature ordnance firing.

The predominant failure modes of the silicon controlled rectifier are open circuits, shorts, and premature firing due to coupling the DC arming voltage from anode to gate during arming of the circuit or premature firing due to noise spikes at the gate after arming the circuit. Parallel redundancy would protect against silicon controlled rectifier opens, but would increase the probability of premature firing in the event

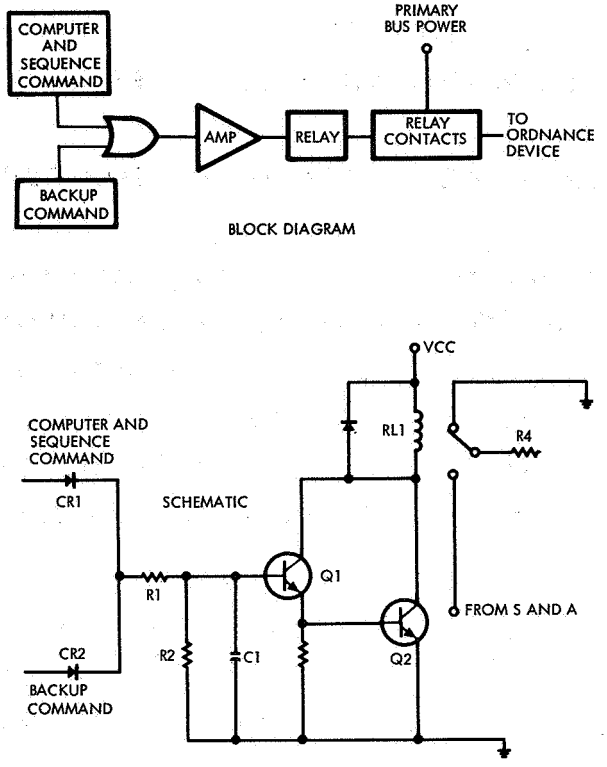


Figure U-1. Typical Relay Ordnance Firing Circuit

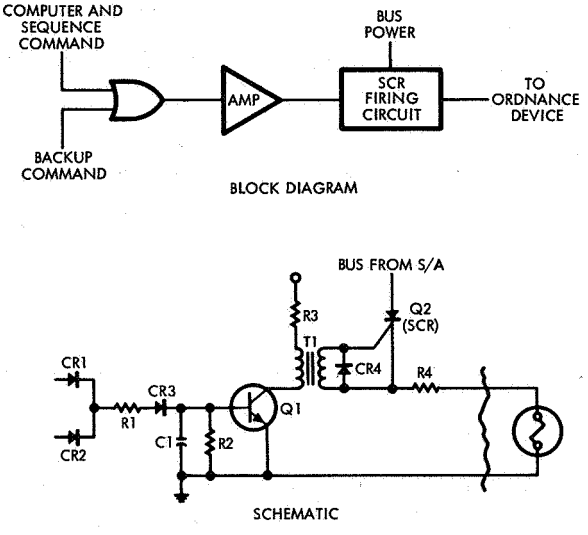


Figure U-2. Typical Solid-State Ordnance Firing Circuit

Table U-1. Solid State Versus Relay Firing Circuit*

	Solid State (SCR + Driver)	Relay + Driver
Size	0.5 - 0.7	1.0
Weight	0.5	1.0
Pwr Standby	Negligible	Negligible
Pwr Diss On	5 watts for 50 msec	2 watts for 50 msec
Vibration Sensitivity	Low	High
EM & I Susceptibility	Requires careful circuit design	Relay - Low Relay driver same as SCR circuit
TRW Experience	Low	All past space programs
Procurement	SCR Transistor	Relay 36 weeks transistors
Relative cost for R1 Parts	$40 SCR cost	$40 relay cost
Thermal	125°C operation	125°C operation
Mounting Limitations	None	Relays have sensitive axis
Safety	No provision for shorting ordnance	Provides shorting and grounding of ordnance before actuation
Other	Can handle repeated high current loads	Contacts degrade with high current loads

*This table presents a comparison of various characteristics associated with solid state and relay firing circuits for spacecraft ordnance. The relay circuit has a large documented history, high reliability and high safety. The SCR circuit is physically smaller, has much less history and does not have the inherent source open circuit and squib shorting features available with a relay.

of shorts, voltage coupling and noise spikes. The overall effect of redundancy may be to increase the probability of circuit malfunction and premature ordnance firing. Existing orbital data on other TRW programs indicates that the reliability of the magnetic latching relay is quite good. The momentary relay does not introduce additional failure modes and a well designed momentary relay should exhibit reliabilities similar to latching relays. The silicon controlled rectifier is not proven in this

application and examination of possible failure modes leads one to the conclusion that most silicon controlled rectifier failures will cause premature ordnance firing. Hence, a silicon controlled rectifier design is not preferred for this application and it is planned that relay circuitry will be utilized.

2. ENERGY STORAGE DEVICES

In the hot bridge wire firing system, the firing currents required are lower than that required by an exploding bridge wire (typical 3.5 amperes versus 1300). The battery for the recommended Voyager spacecraft is able to provide a peak current capability of 100 amperes. Therefore, for hot bridge wire explosive devices, capacitors will not be necessary to augment the battery capacity. Some transients will be induced upon the battery bus due to electro-explosive device actuation, but this problem will be alleviated in the design of the cabling and inputs to other units on the bus.

The condition of an electro-explosive device shorting and imposing a permanent load on the battery bus is prevented by safe-arm device, firing circuit opening, and series resistor protection.

3. INITIATOR TRADEOFFS

A study was made comparing the total system characteristics of hot bridge wire and exploding bridge wire electropyrotechnic cartridges (or initiators). Table U-2 lists the various characteristics of the two systems.

The hot bridge wire type requires a much simpler, smaller and lighter total system. This is primarily because exploding bridge wire devices require complex electrical power supplies matched to each type of exploding bridge wire, bulky coaxial cables for transmission of electrical firing signals, and mechanical adapters at each load device. No exploding bridge wire systems have been used in TRW spacecraft programs. The electrical complexity results from the bulky DC/DC converter required to develop high voltages, from the very bulky cable required to transmit the high current to the initiator, from the large high-voltage capacitors required to store the energy for the firing current and from the complex high-voltage switching devices required for controlling

Table U-2. Characteristics of Electro-explosive Device Hot Wire Versus Exploding Bridge Wire*

	Typical Hot Wire	Typical Exploding Bridge Wire
Typical Energy	0.2 watt seconds	1.69 watt seconds
Reliability	PT1-11 has a demonstrated reliability of 0.9997	Insufficient data
Lead lengths	Not critical	Requires matched transmission line
Interconnect Cable	Twisted pair shielded required	Bulky coaxial cable required
Initiating circuit requirements	Simple switch closure	High voltage supply high voltage switch matched power supplies
Explosive Charge	Uses sensitive and non-sensitive charge	Generally nonsensitive charge
Pressure buildup	Slow	Rapid
Normal use	Gas pressure generation	Detonation
Normally used for gas pressure generation	Yes	No
Adaptable to gas pressure operated systems	Yes	Requires additional adaptation hardware
Complexity for planned Voyager application	Low	Large (high)
Flight qualified components available	Yes	No
Can be tested	Yes	No

*This table presents a comparison of features associated with hot bridge wire and exploding bridge wire pyrotechnic devices. The exploding bridge wire device requires a much more complex control system.

the high-voltage firing current. All the high voltage equipment would need protection against the effects of humidity and other preflight conditions.

In addition, because of the added electrical circuitry and mechanical adapters, the reliability is reduced. Also most exploding bridge wire initiators contain a series break or gap, which makes preflight testing very difficult.

It is concluded that a hot bridge wire system is more desirable than an exploding bridge wire system.